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Power Converter Topologies: Is there something new?

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>20 years R/D & Academic Experience

- RDA Co, Belgrade, Serbia
- CESET, Italy
- PDL Electronics, Ltd., Napier, New Zealand.
- Schneider Toshiba Inverter Europe, Pacy-Sur-Eure, France,
- General Electric Global Research, Munich, Germany.
- HUAWEI Technologies, Düsseldorf GmbH, Munich, Germany,
- Centre of Power Electronics and Drives, C-PED Lab., Roma TRE University, Italy.
- Innsbruck Power Electronics Laboratory (***i-PEL***), the University of Innsbruck, Austria.

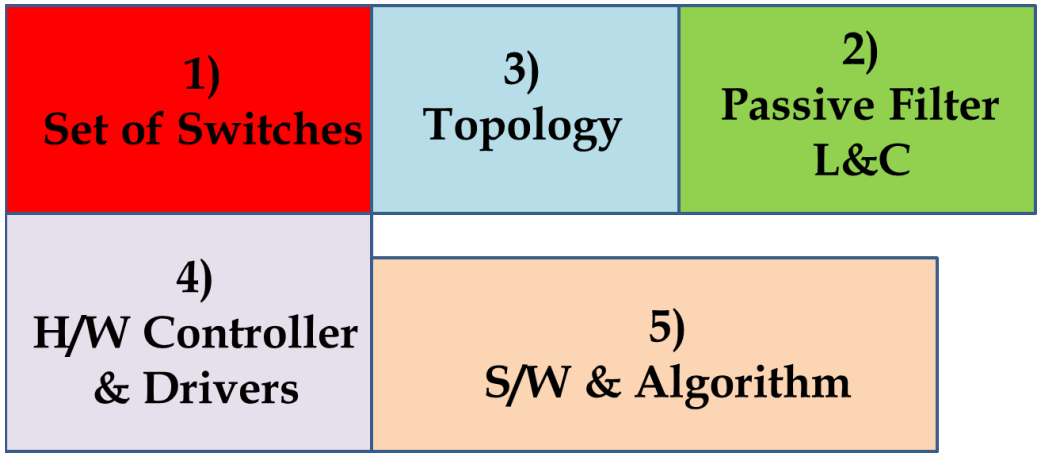
What is a Power Converter?

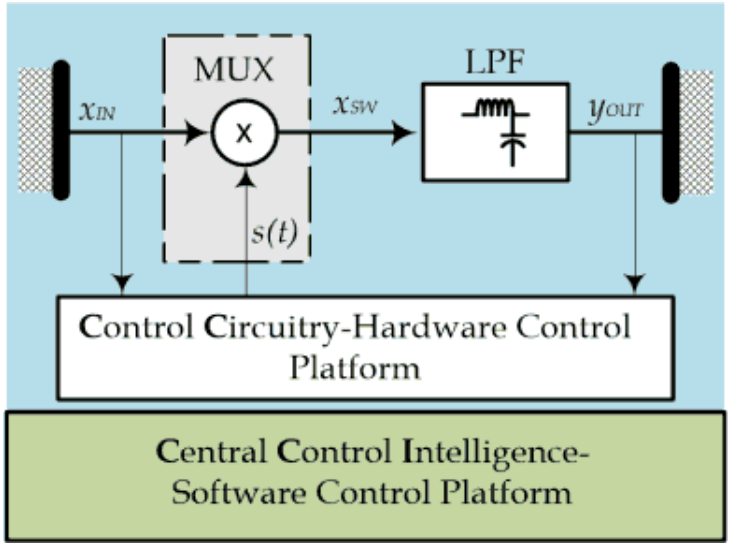
Power Converter is a device that converts one electric quantity into another

- **BUT, without (significant) losses**

Main 5 Ingredients

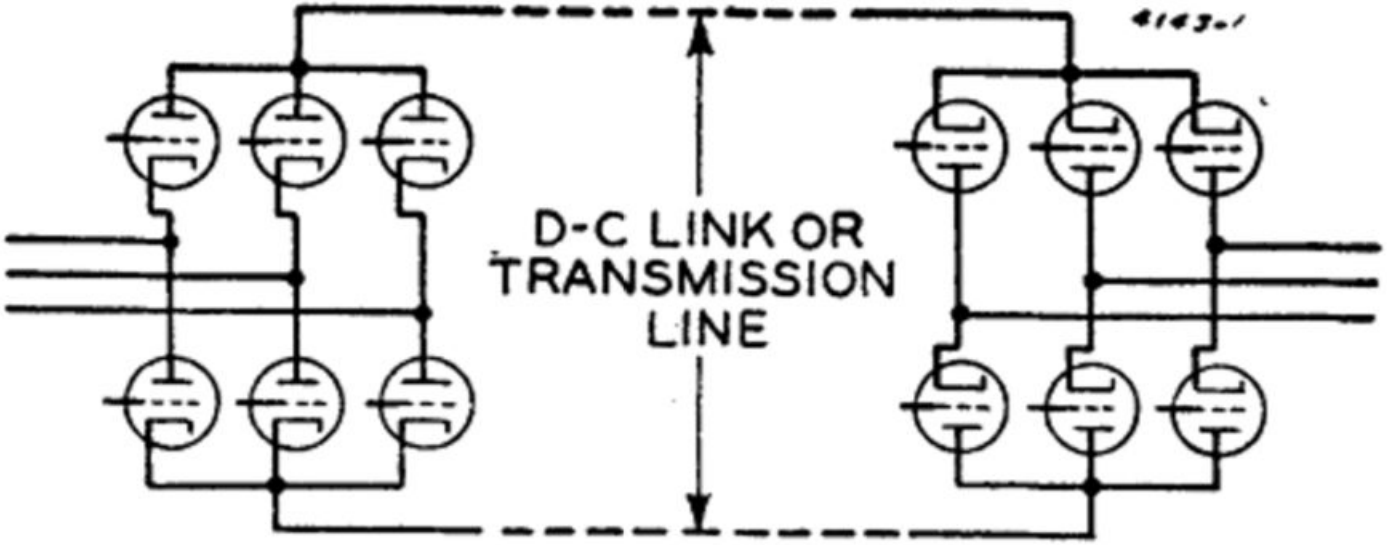
1) Set of Switches (Power semiconductor)
2) Passive LC Filter
3) **Topology**
4) H/W Controller
5) S/W & Control

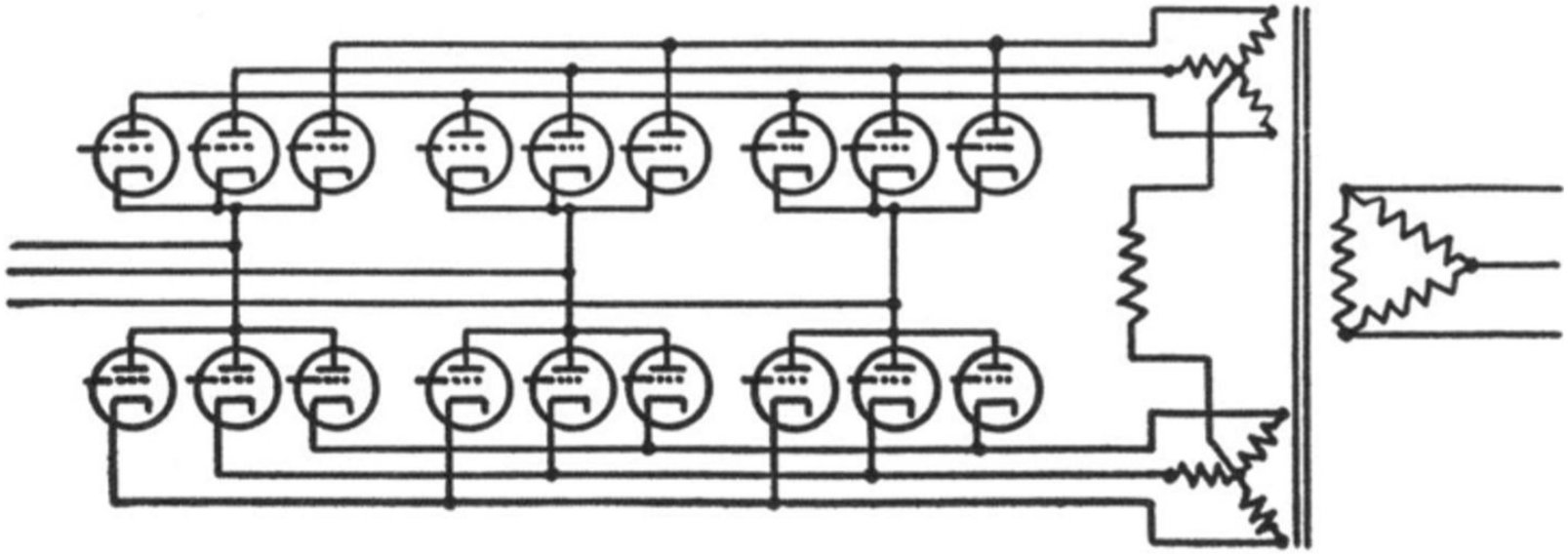


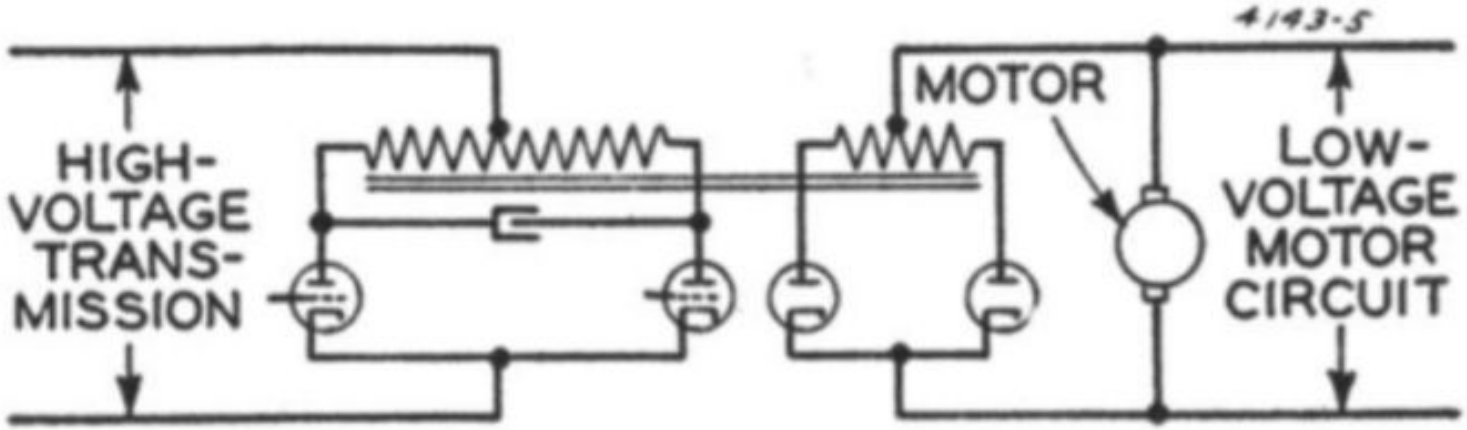


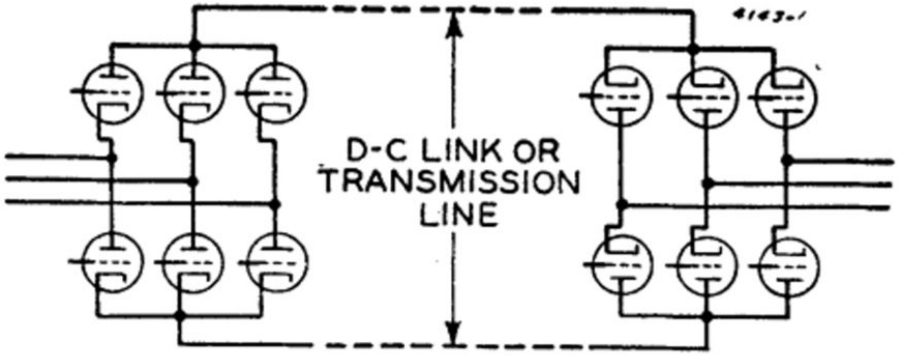
3) Topology?

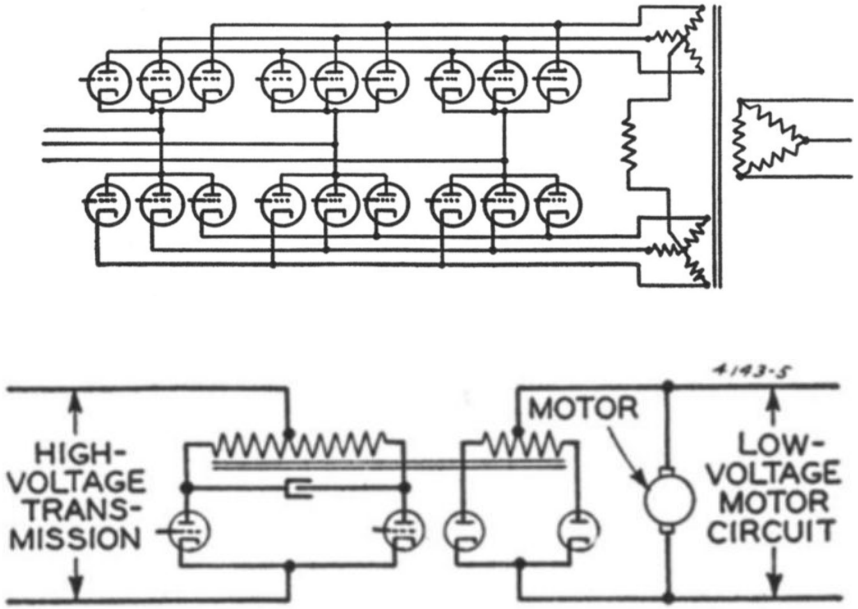
- Is there a magic topology that will solve all our issues?
- Is there something new?
- Will something new come soon?





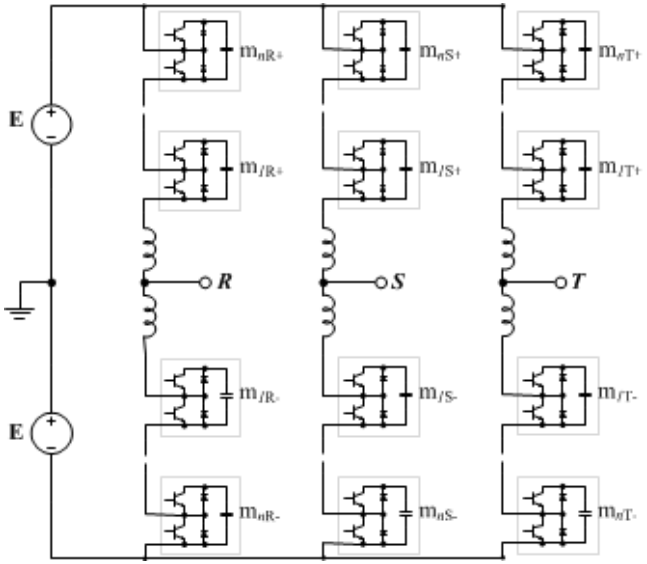

4143-5
HIGH-
VOLTAGE
TRANS-
MISSION
MOTOR
LOW-
VOLTAGE
MOTOR
CIRCUIT

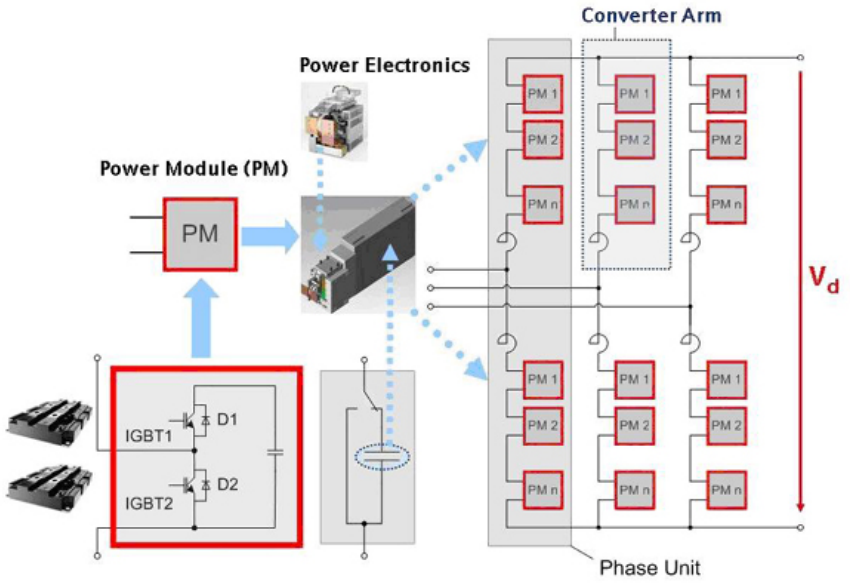




E. Alexanderson, "**History and development of the electronic power converter**", Trans. of the American Institute of Electrical Engineers (**Volume: 63 , Issue: 9 , Sept. 1944**)

Modular **M**ultilevel **C**onverter is somehow new (already 15 years old)





We need to explore existing topologies and use them in different way

a) Partial Power Processing Converters

b) Current Source Converters

c) Multi-Cell & Multi-Level Converters, and

d) Quantum Mode Resonant Converters

We need to explore existing topologies and use them in different way

a) Partial Power Processing Converters

b) Current Source Converters

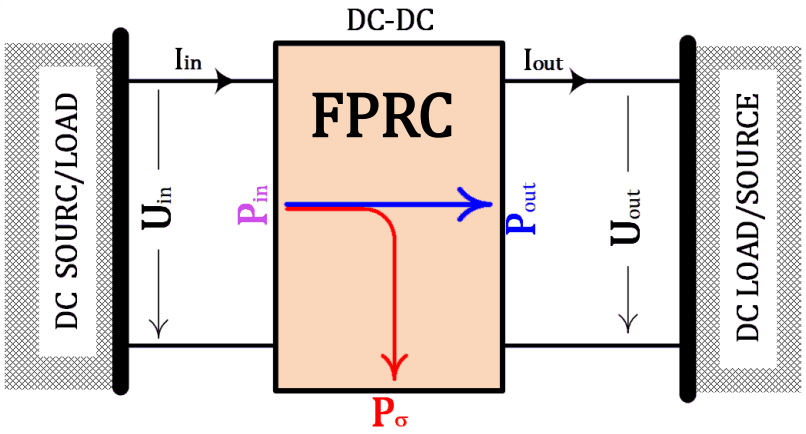
c) Multi-Cell & Multi-Level Converters, and

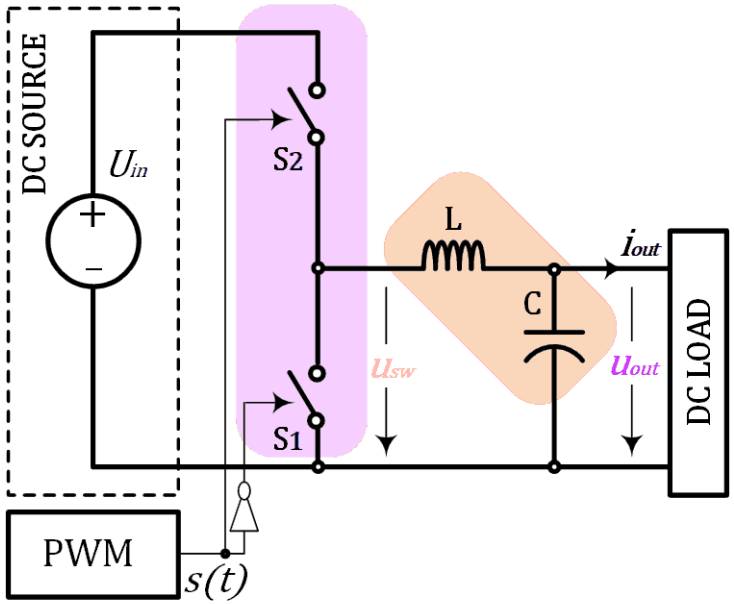
d) Quantum Mode Resonant Converters

Partial Power Rated Converters

-Process a Fraction of Power instead of processing Full Power-

Partial Power Rated Converters

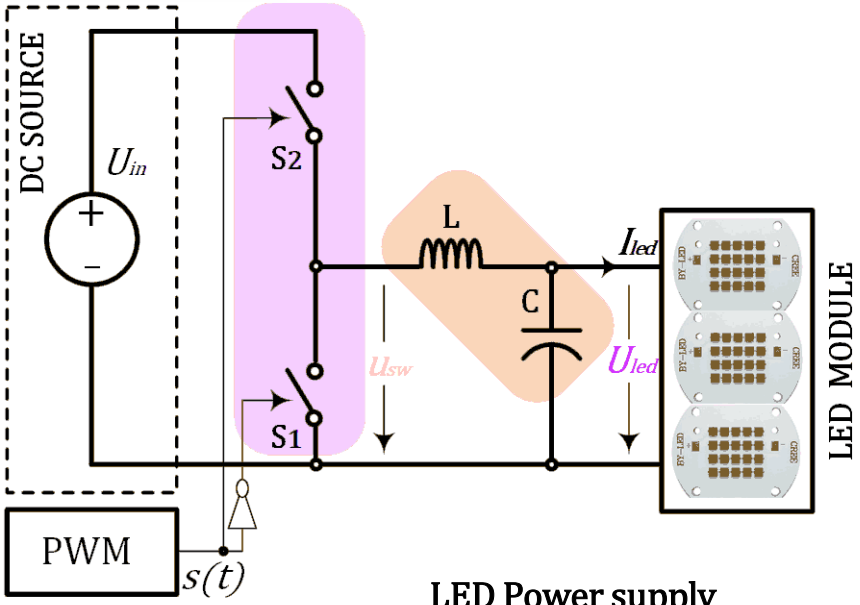




Full Power Rated Converter

- The converter is handling full voltage and full current
- The output (can be) controlled in the range 0-to-100%
- Active devices apparent power rating
- LC Filter apparent power rating

Partial Power Rated Converters



LED Power supply

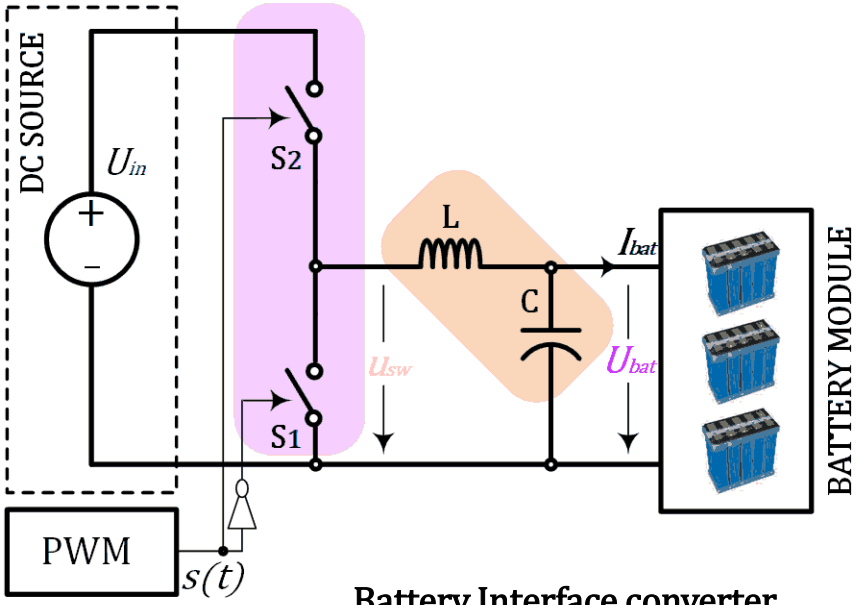
$U_{in} = 54$ [V]

$U_{led} = U_n \pm 10[\%] = 44 \sim 52[V]$

$\boldsymbol{U_{sw} = k_u\, U_{in} = 75\ [V]}$

$\boldsymbol{I_{sw} = k_i I_{led}}$

$\boldsymbol{L \sim U_{in}}$



Battery Interface converter

$U_{in} = 750$ [V]

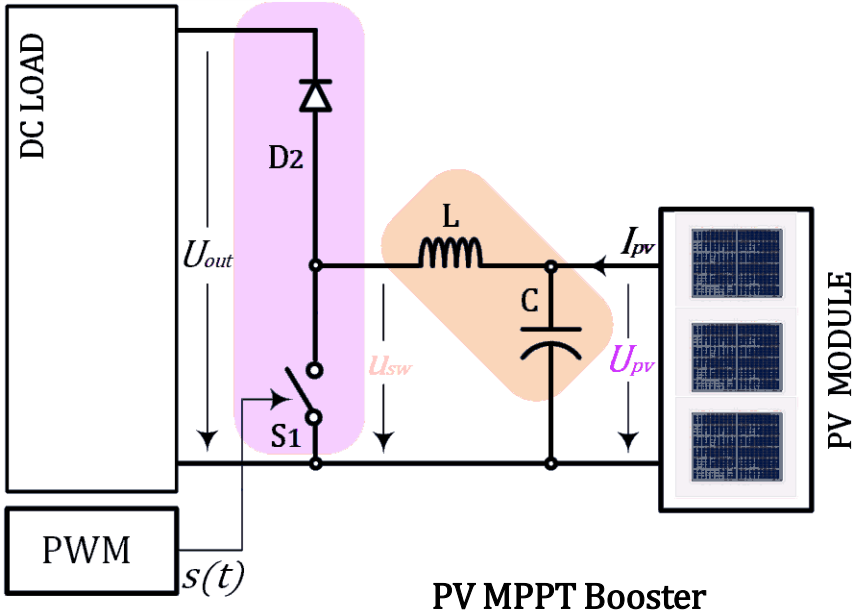
$U_{bat} = U_{bat(n)} \pm 15\%$[V]

$\boldsymbol{U_{sw} = k_u\, U_{in} = 1200\ [V]}$

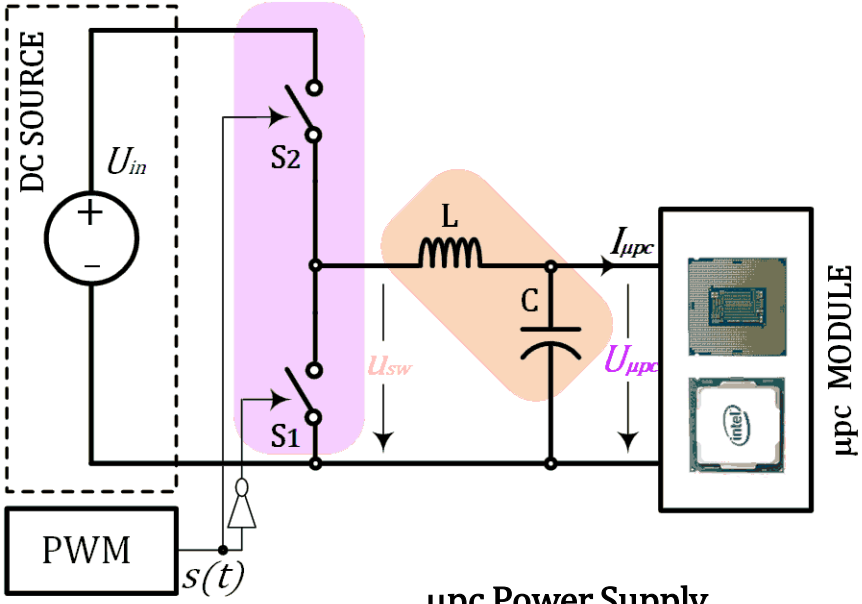
$\boldsymbol{I_{sw} = k_i I_{bat}}$

$\boldsymbol{L \sim U_{in}}$

Partial Power Rated Converters



PV MPPT Booster

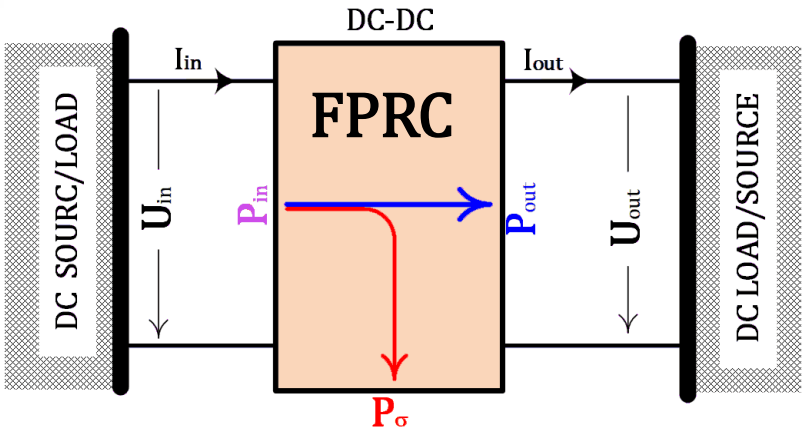


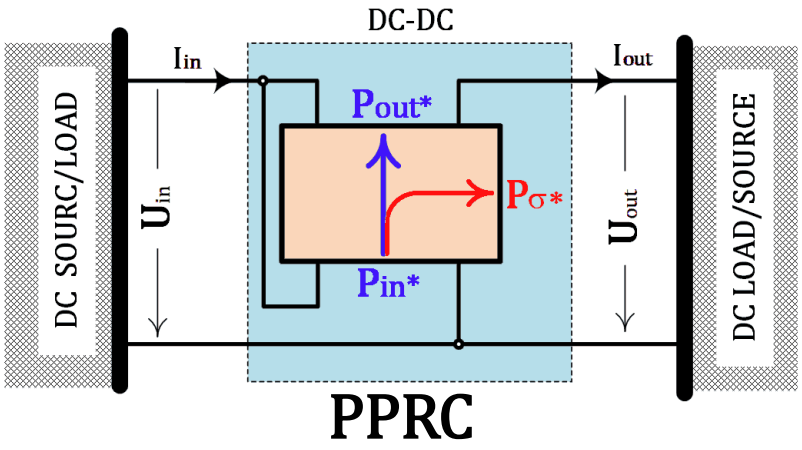
μpc Power Supply

$U_{out} = 850$ [V]
$U_{pv} = 500 \sim 850[V]$
$\boldsymbol{U_{sw} = k_u\, U_{in} = 1200\ [V]}$
$\boldsymbol{I_{sw} = k_i I_{pv}}$
$\boldsymbol{L \sim U_{in}}$

$U_{in} = 12$ [V]
$U_{\mu pc} = 1[V]$
$\boldsymbol{U_{sw} = k_u\, U_{in} = 30\ [V]}$
$\boldsymbol{I_{sw} = k_i I_{\mu pc}}$
$\boldsymbol{L \sim U_{in}}$

Partial Power Rated Converters





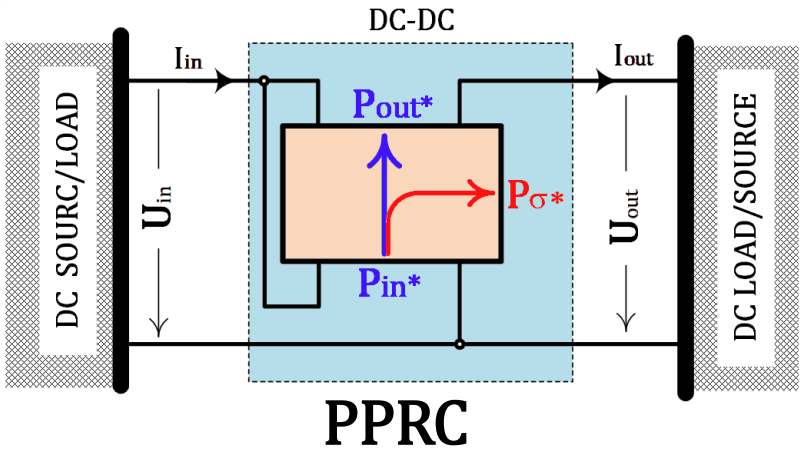
Full Power Rated Converter

- The converter is handling full voltage and full current
- The output (can be) controlled in the range 0-to-100%
- Active devices apparent power rating
- LC Filter apparent power rating

Partial Power Rated Converter

- The converter is handling a fraction of voltage or current
- The output (can be) controlled in narrow range
- Active devices apparent power rating
- LC Filter apparent power rating

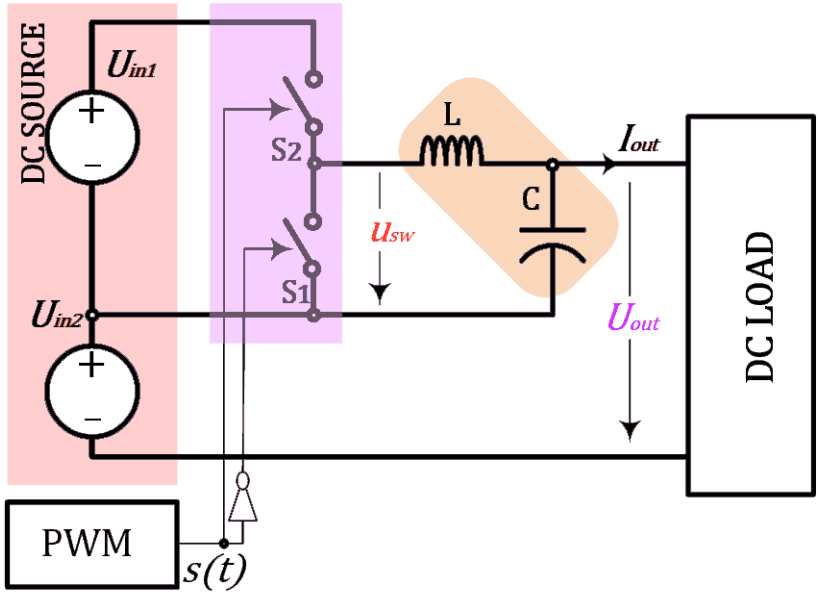
Partial Power Rated Converters



PPRC

Partial Power Rated Converter

- The converter is handling a fraction of voltage or current
- The output (can be) controlled in narrow range
- Active devices apparent power rating
- LC Filter apparent power rating



$U_{in} = 750$ [V]

$U_{bat} = U_{bat(n)} \pm 15\%$[V]

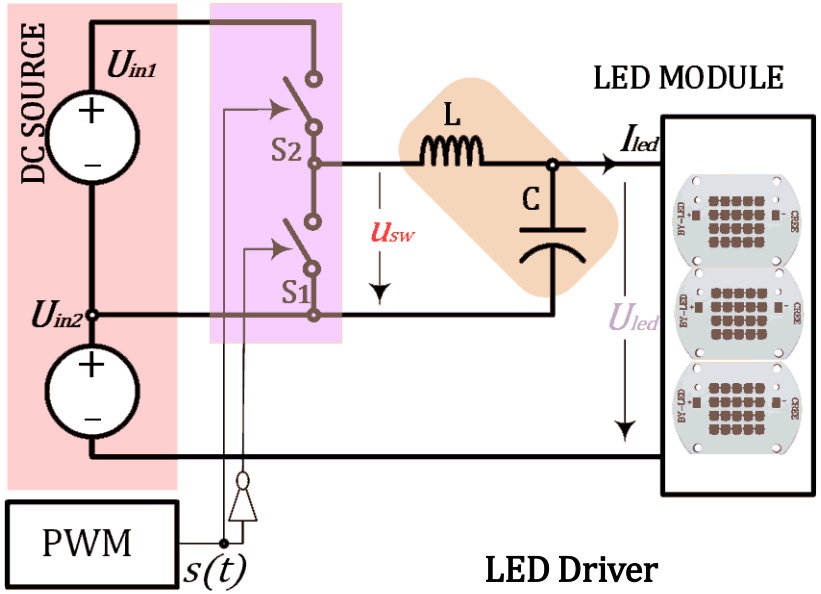
$U_{in1} = U_{in2} = 375$ [V]

$\boldsymbol{U_{sw} = k_u\, U_{in1} = 650\ [V]}$

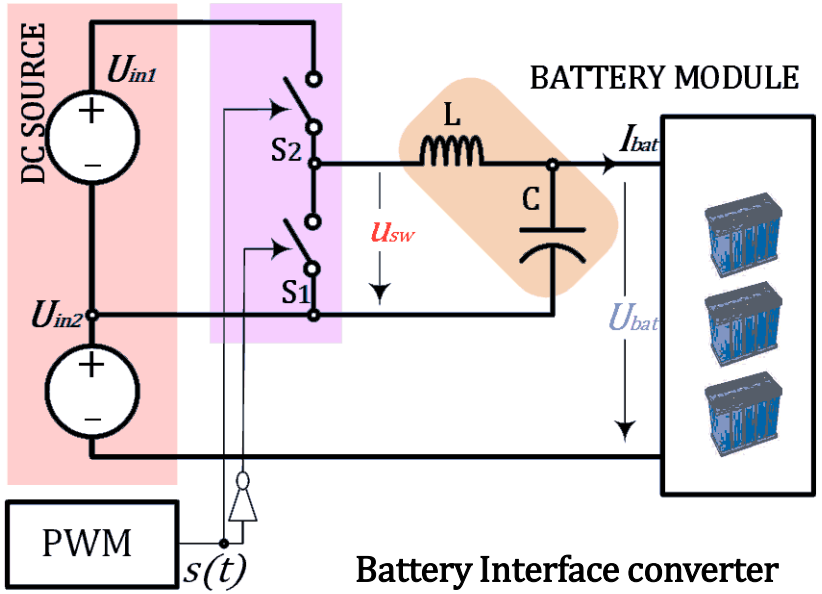
$\boldsymbol{I_{sw} = k_i I_{bat}}$

$\boldsymbol{L \sim U_{in1}}$

Partial Power Rated Converters



LED Driver

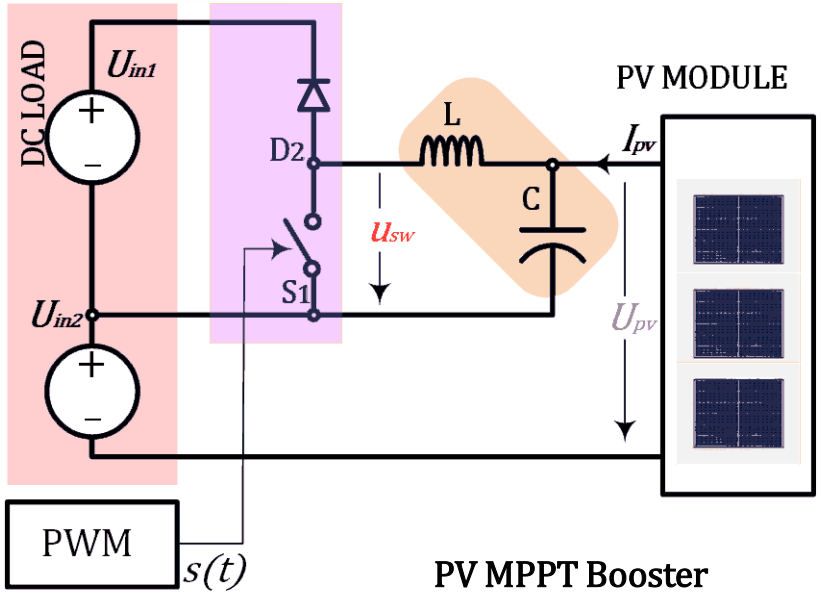


Battery Interface converter

$U_{in} = 54$ [V]
$U_{led} = U_n \pm 10[\%] = 44 \sim 52[V]$
$U_{in1} = U_{in2} = 26$ [V]
$\boldsymbol{U_{sw} = k_u\, U_{in1} = 40\ [V]}$
$\boldsymbol{I_{sw} = k_i I_{led}}$
$\boldsymbol{L \sim U_{in1}}$

$U_{in} = 750$ [V]
$U_{bat} = U_{bat(n)} \pm 15\%$[V]
$U_{in1} = U_{in2} = 375$ [V]
$\boldsymbol{U_{sw} = k_u\, U_{in1} = 650\ [V]}$
$\boldsymbol{I_{sw} = k_i I_{bat}}$
$\boldsymbol{L \sim U_{in1}}$

Partial Power Rated Converters



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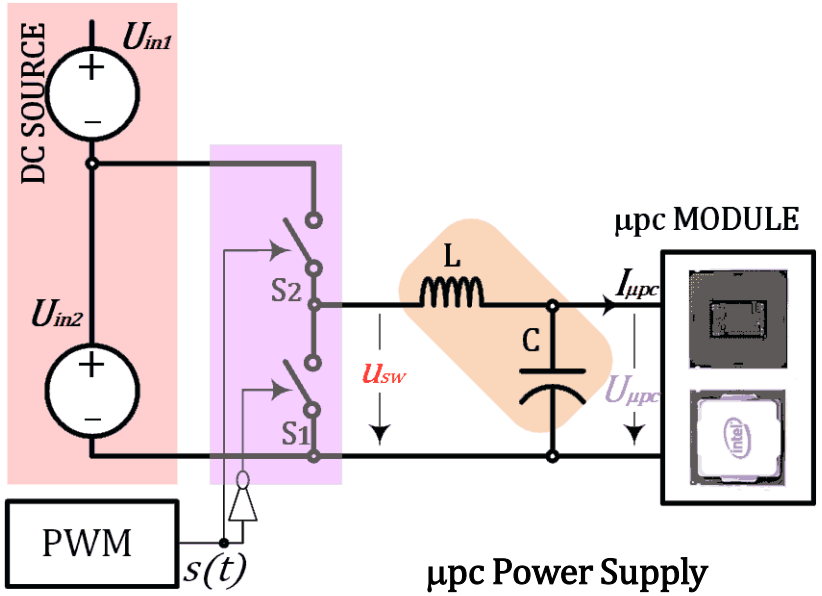
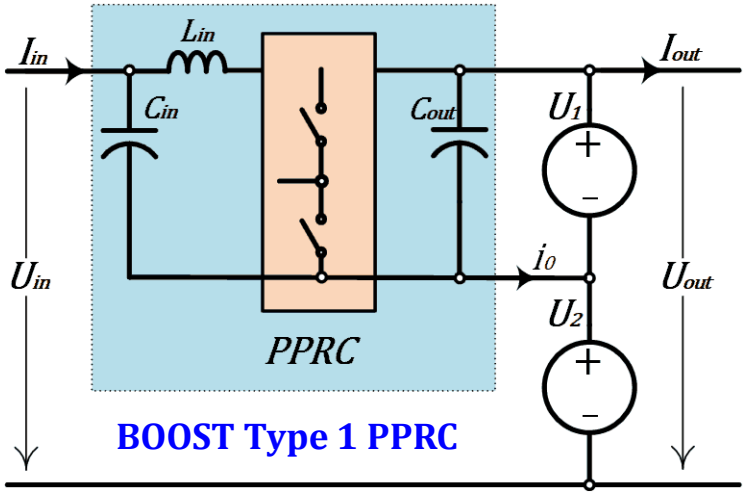


µpc Power Supply

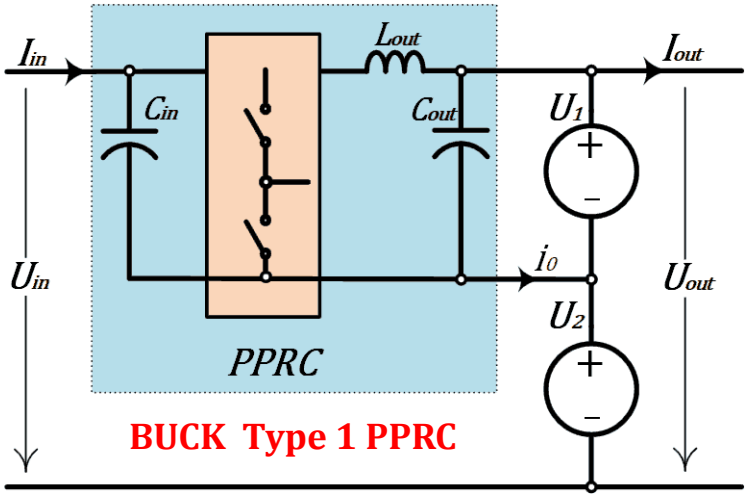
$U_{out} = 850$ [V]
$U_{pv} = 500 \sim 850[V]$
$U_{in1} = U_{in2} = 425$ $[V]$
$\boldsymbol{U_{sw} = k_u U_{in1} = 650\ [V]}$
$\boldsymbol{I_{sw} = k_i I_{pv}}$
$\boldsymbol{L \sim U_{in1}}$

$U_{in} = 12$ [V]
$U_{\mu pc} = 1[V]$
$U_{in1} = U_{in2} = 6$ $[V]$
$\boldsymbol{U_{sw} = k_u U_{in1} = 20\ [V]}$
$\boldsymbol{I_{sw} = k_i I_{\mu pc}}$
$\boldsymbol{L \sim U_{in1}}$

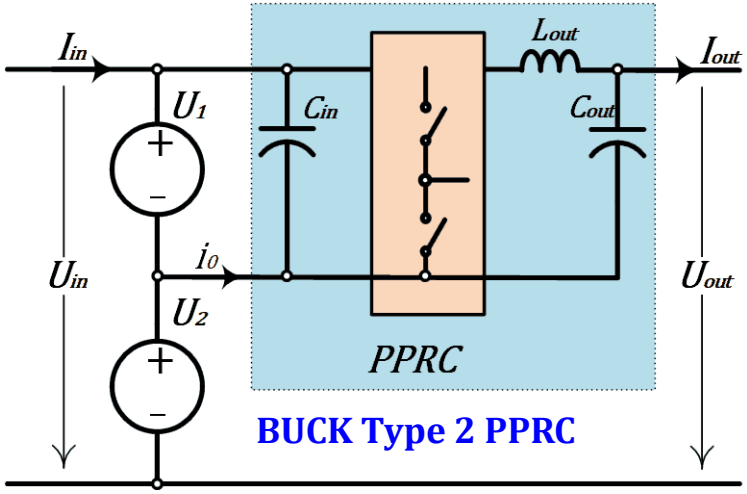
Partial Power Rated Converters



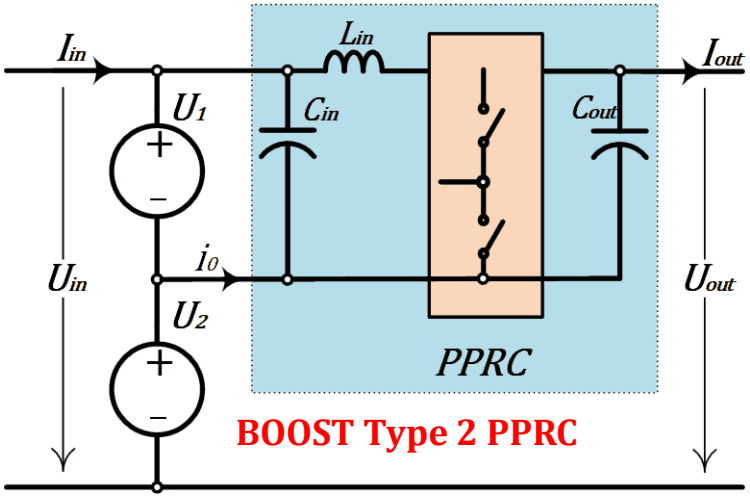
BOOST Type 1 PPRC



BUCK Type 1 PPRC



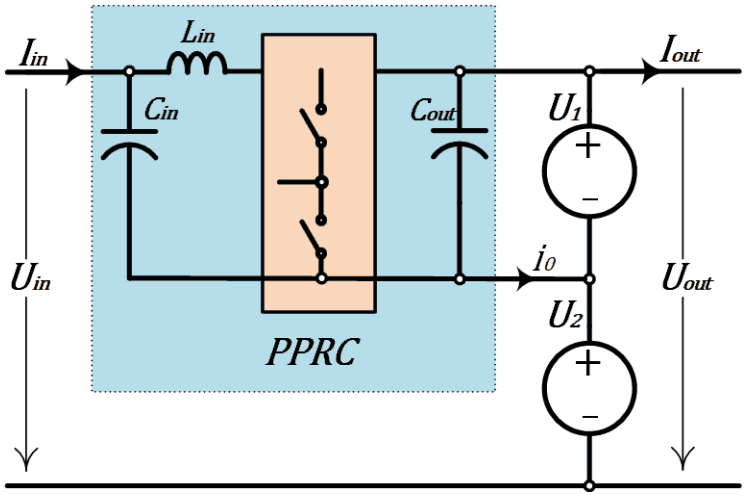
BUCK Type 2 PPRC



BOOST Type 2 PPRC

Partial Power Rated Converters

Why PPRC is (should be) better than the FPRC?



Boost Type 1 PPRC

- The BSC DC Bus Voltage is a fraction of the total DC Bus voltage $U_1 = U_{out} k_1 = U_{sw}$

a) Switch and diode voltage rating is reduced
   i. Reduced on-state resistance
      $R_{ds} \sim U_{sw}^{2,5}$
   ii. Better switching
      Different switch technology
      IGBT → MOSFET
      SiC → GaN…

b) The inductor flux is reduced
   i. Smaller and more efficient Inductor(s)

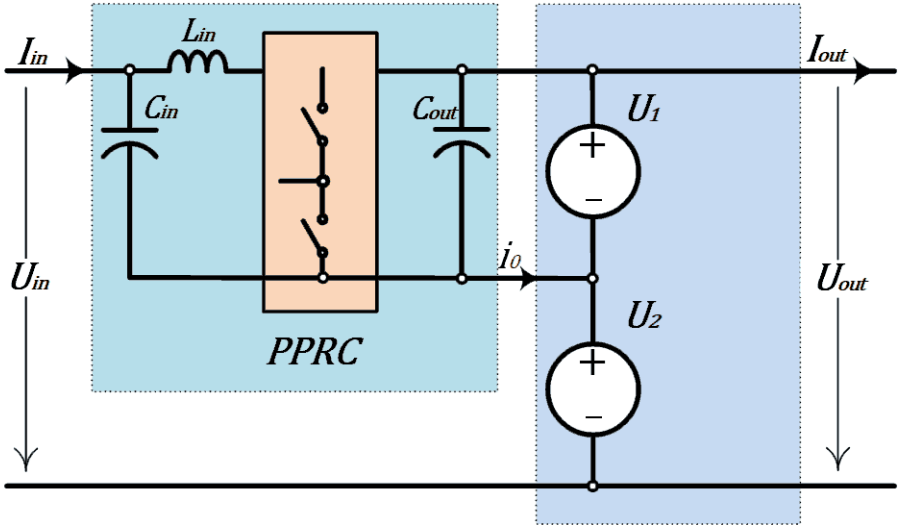
c) Input filter Capacitor voltage reduced
   i. Smaller capacitor

Partial Power Rated Converters

The following has been assumed:

a) The Output (Input) is spilt voltage source
   - $U_1 = k_1 U_{out}$
   - $U_2 = (1 - k_1)\, U_{out}$

b) The voltages ratio is constant regardless on the input/output current variation



- In some specific applications the input (output) source (load) is (could be) split voltage source
  - PV string
  - Battery string..

Partial Power Rated Converters

The following has been assumed:

a) The Output (Input) is spilt voltage source
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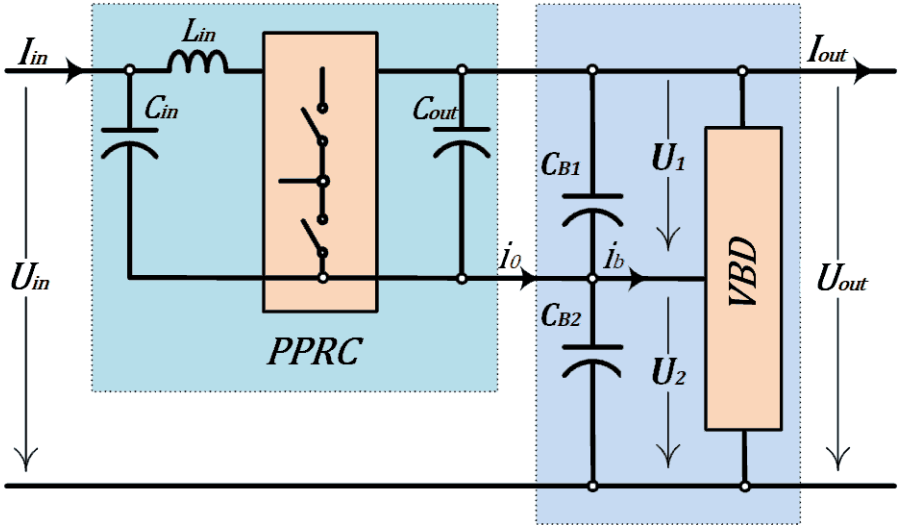
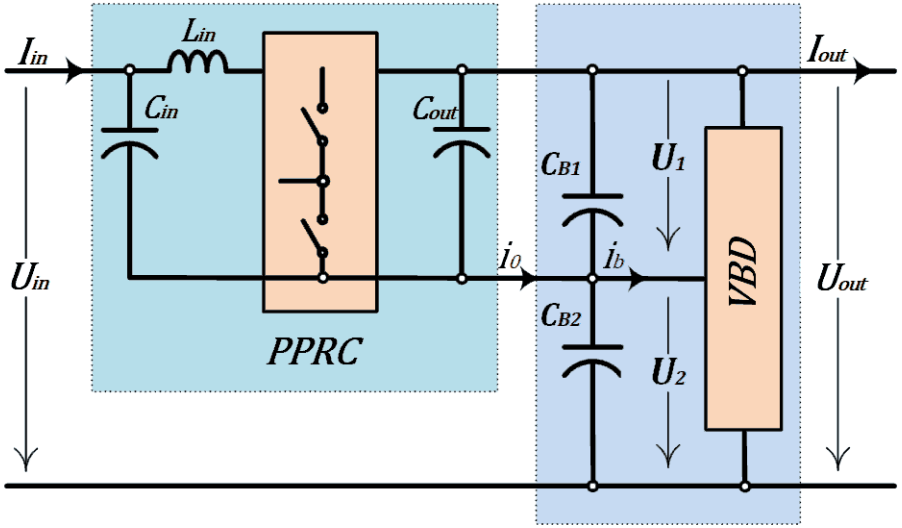


- However, in most of applications that is not case
  - Single voltage source or passive load that must be spilt into two voltage sources..
  - The DC BUS capacitor is split into two series connected capacitors
    - Similar to Three-Level NPC and T type converters!

Partial Power Rated Converters

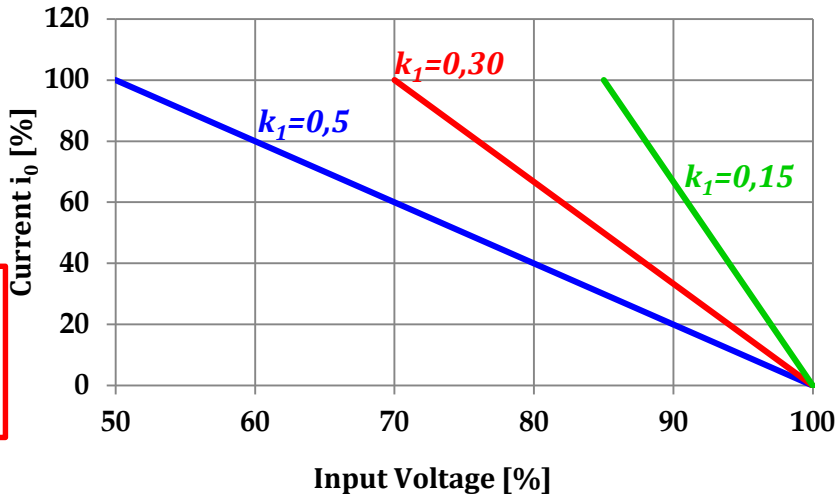
- The DC BUS spilt into two cells
  - $C_{B1}, C_{B2} \rightarrow U_1, U_2$



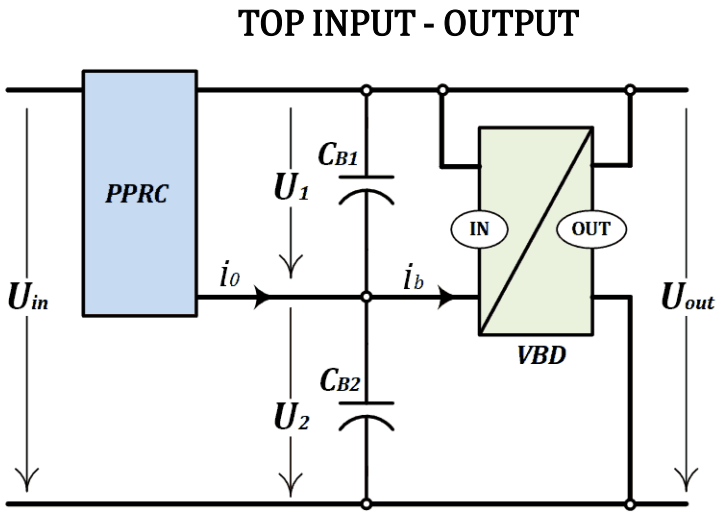
No Meal for Free!

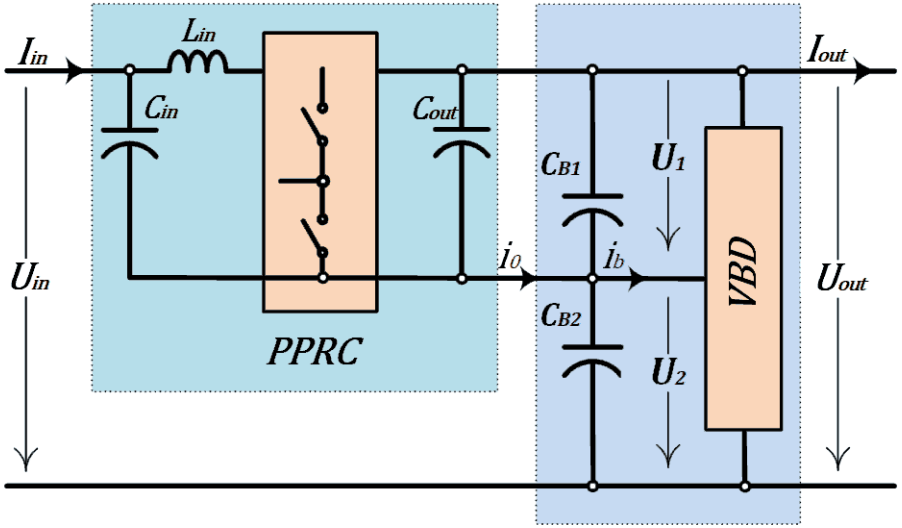
- The PPRC injects an average current i_0 into the dc bus caps. mid point!
- The caps. average current must be zero…Steady State… !
- The current i_0 must be canceled by i_b current!

$$i_0 = i_b = I_{in}\frac{U_{out} - U_{in}}{k_1 U_{out}} \quad \& \quad U_1 = k_1 U_{out}$$



Partial Power Rated Converters

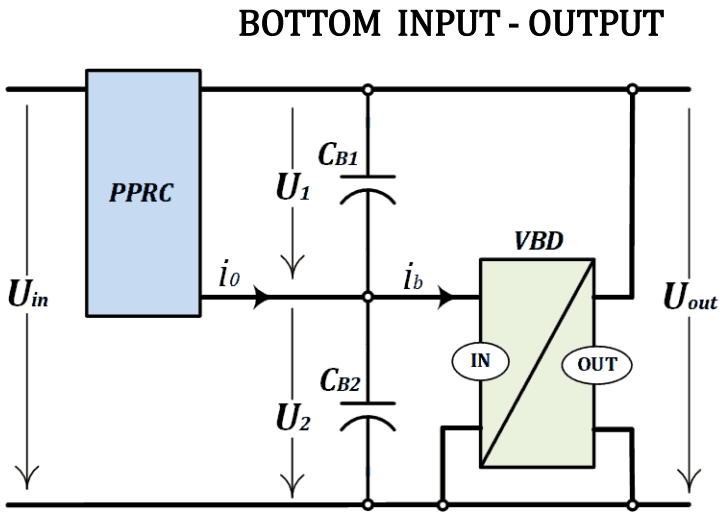


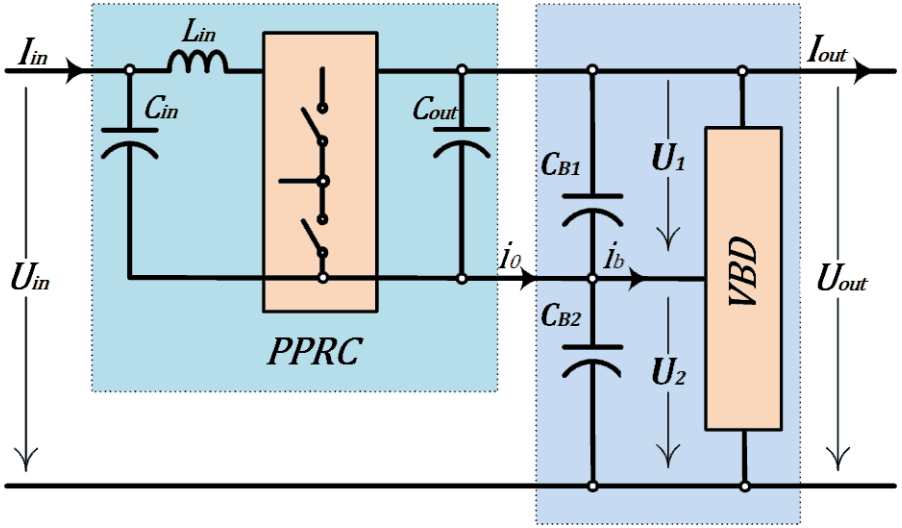


Voltage Balancing Device (VBD)

a) Two Terminal Device (INPUT & OUTPUT)
b) Uni-Directional or Bi-Directional
c) Isolated or Non-Isolated

Partial Power Rated Converters





Voltage Balancing Device (VBD)

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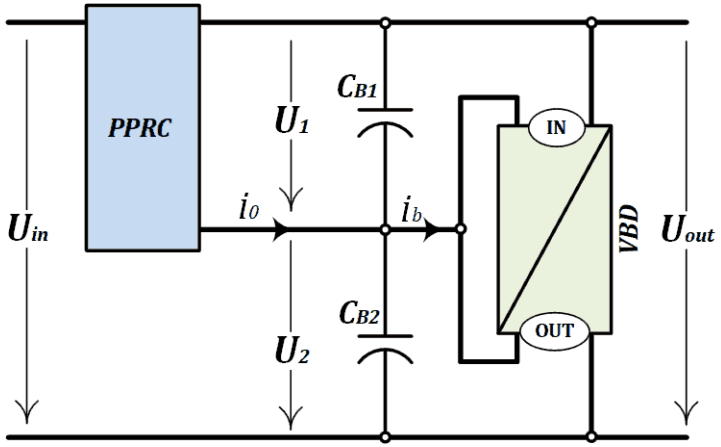
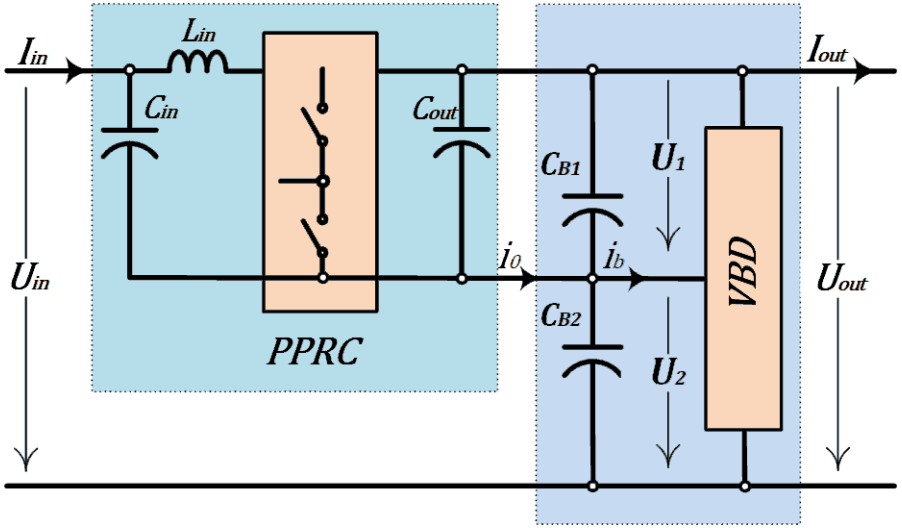
Partial Power Rated Converters

TOP INPUT – BOTTOM OUTPUT





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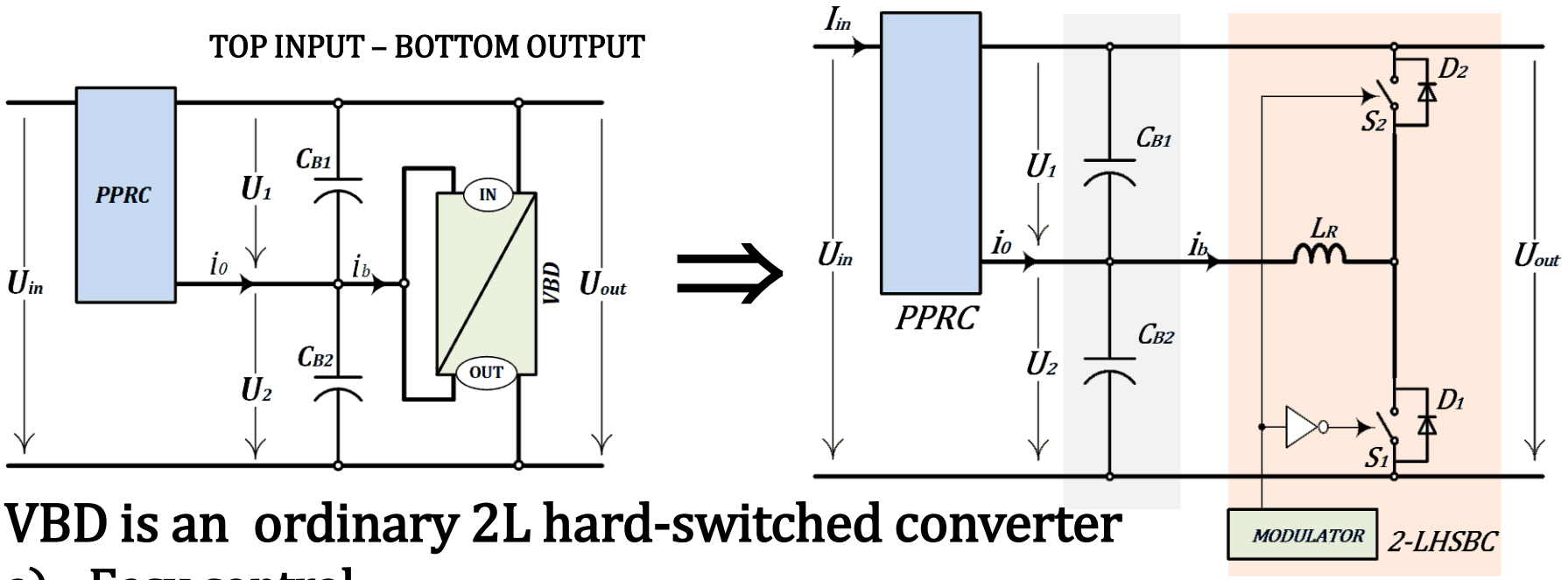


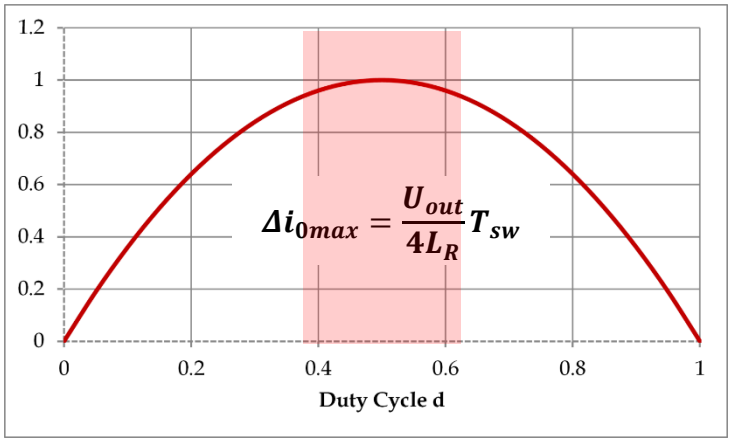
VBD is an ordinary 2L hard-switched converter

a) Easy control
   - $U_1 = (1-d)U_{out}$ & $d = 1 - k_1$

b) Large Inductor L_R
   - The worst case condition d~0,5

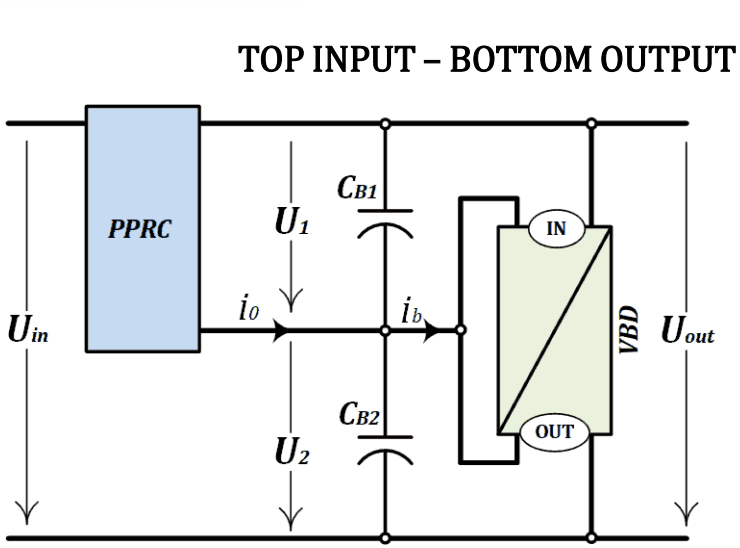
c) Full voltage rated switches & diodes

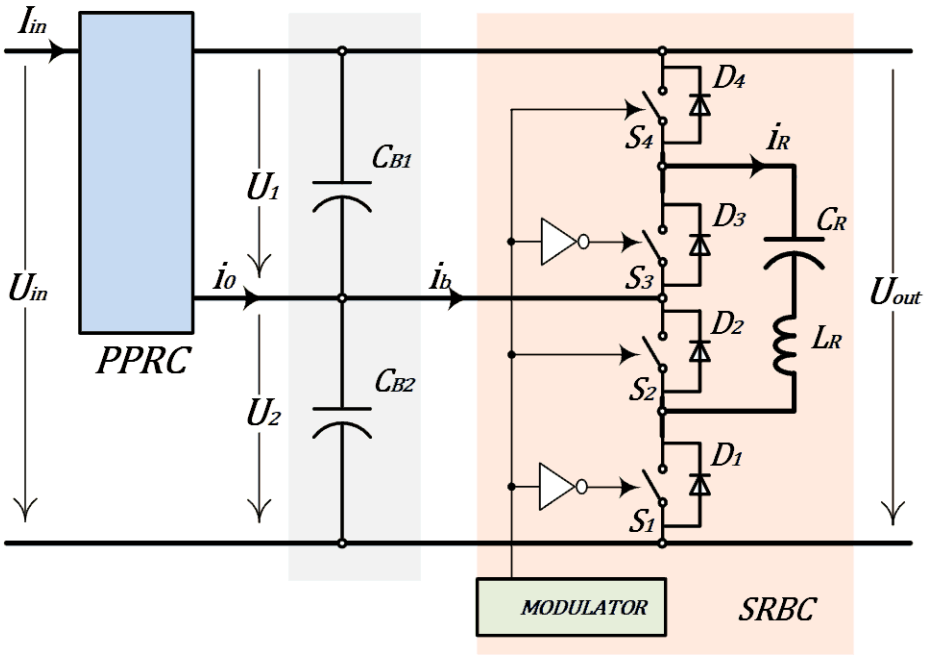
d) Switching losses



Partial Power Rated Converters

TOP INPUT – BOTTOM OUTPUT





1. **Petar J. Grbović**, Philippe Delarue and Philippe Le Moigne, "A novel three-phase diode boost rectifier using hybrid half-DC-BUS-voltage rated boost converter," *IEEE Trans. Industrial Electronics,* Vol. 58, No. 4 pp. 1316-1329, April 2011.
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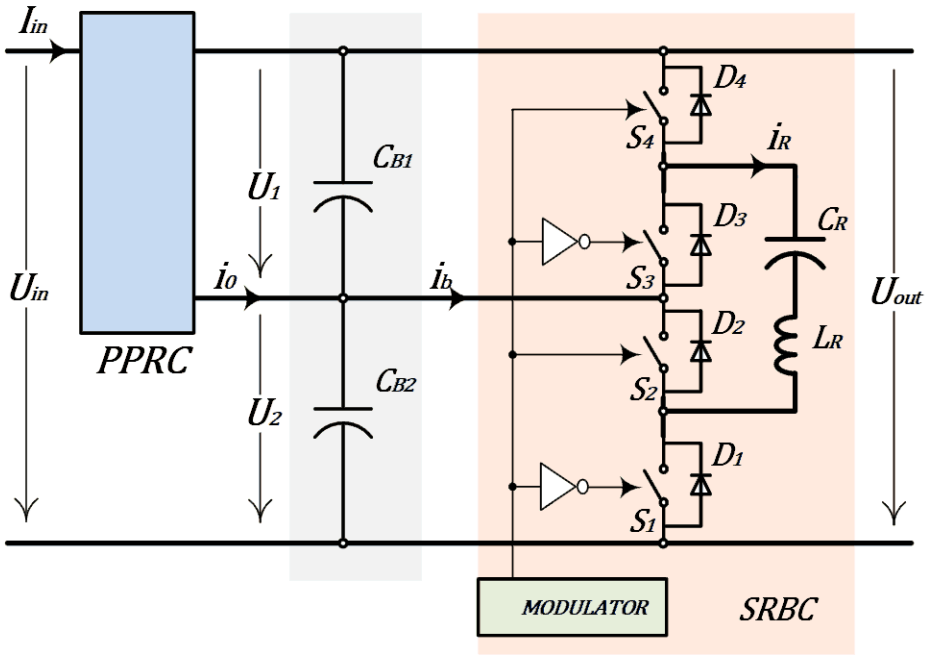
Partial Power Rated Converters

Series Resonant Voltage Balancing Device (SR-VBD)

a) Two switching cells (1,2 & 3,4) connected across bottom and top dc bus capacitors
b) A resonant tank (L_R C_R) connected between cells
c) The cells duty cycle $d \cong 0,5$

d) Switches & diodes voltage rating is half of the output voltage
e) Zero current switching
f) No large inductors required
g) More devices and gate drivers
h) Resonant capacitor current stress



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- Voltage Balancing is a MUST and it is additional burden in most of the applications

Partial Power Rated Converters

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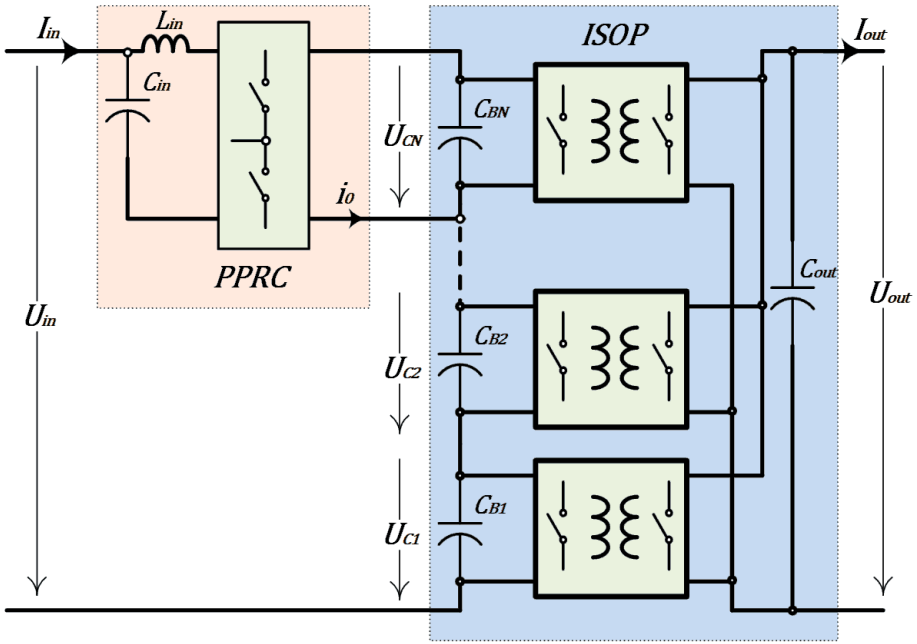
- In some specific applications, the voltage balancing device can be an intrinsic feature of the converter



- Input Series Output Parallel (ISOP) ISO Converters
- One Cell can be used as a VBD
  - No additional VBD is required
  - Power distribution is not symmetrical between all cells

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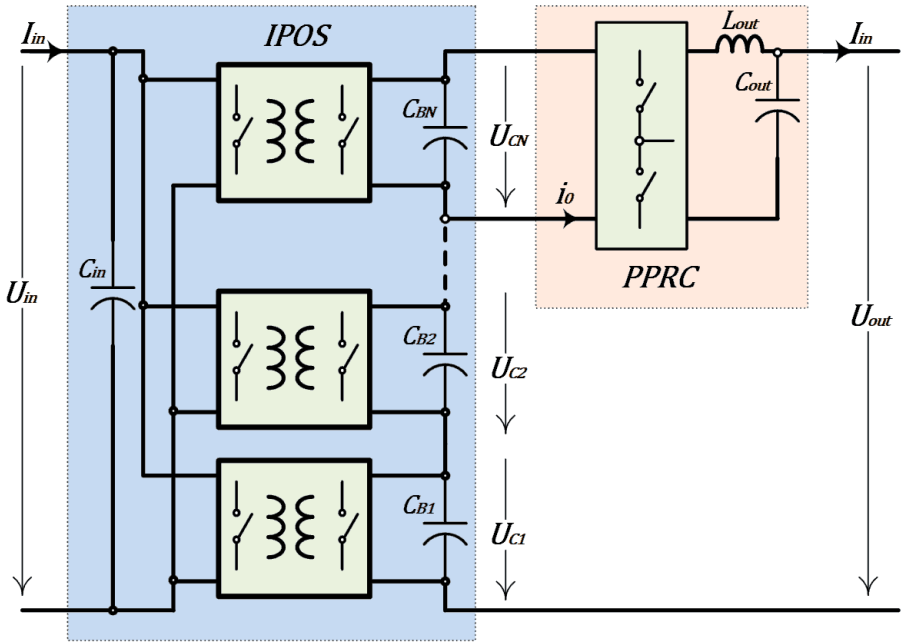

- Input Series Output Parallel (ISOP) ISO Converters
- The same concept can be used with Input Parallel Output Series (IPOS) ISO Converters
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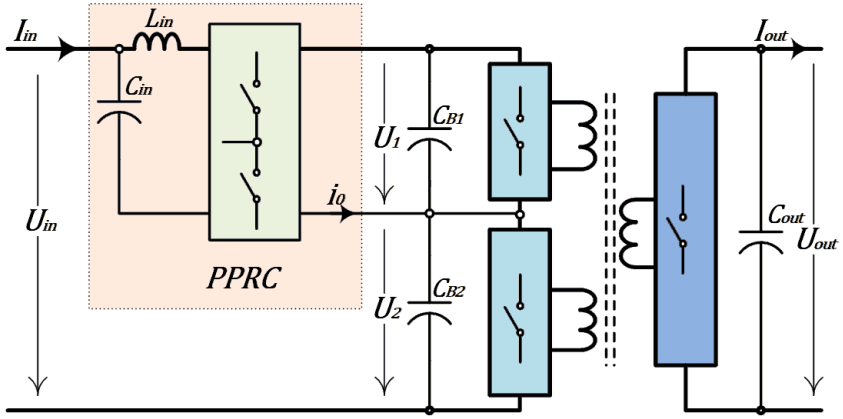

- Similar concept can be used with Single Transformer Multi-Input ISO Converters
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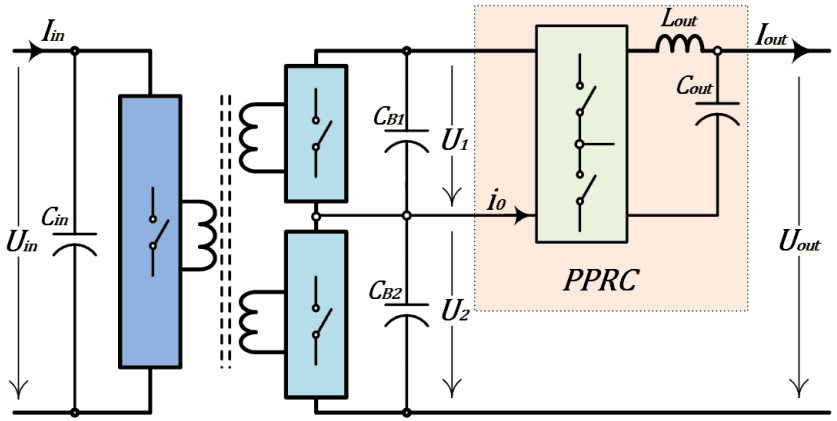

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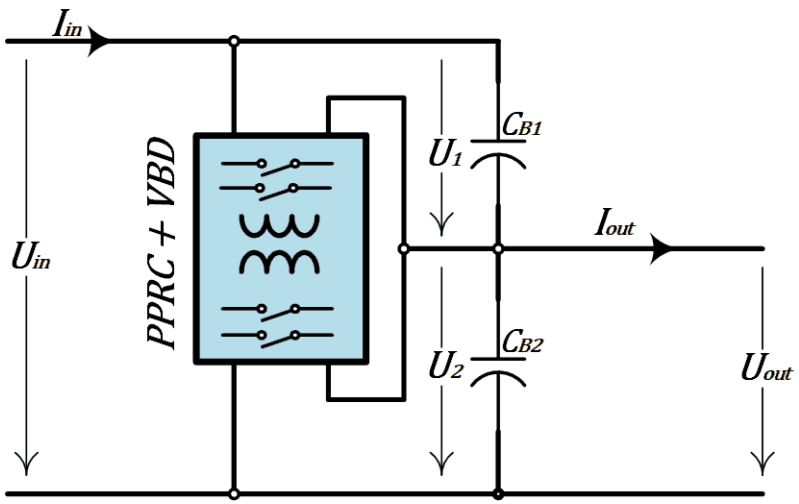

- Similar concept can be used with TOP Input-BOTTOM Output ISO VBD
  - U_1 to U_2 voltage ratio is not constant
  - $U_{out} < U_{in}$ (BUCK)
  - The converter is PPRC + VBD
    - DAB
    - SRC
    - LLC
    - PS FB

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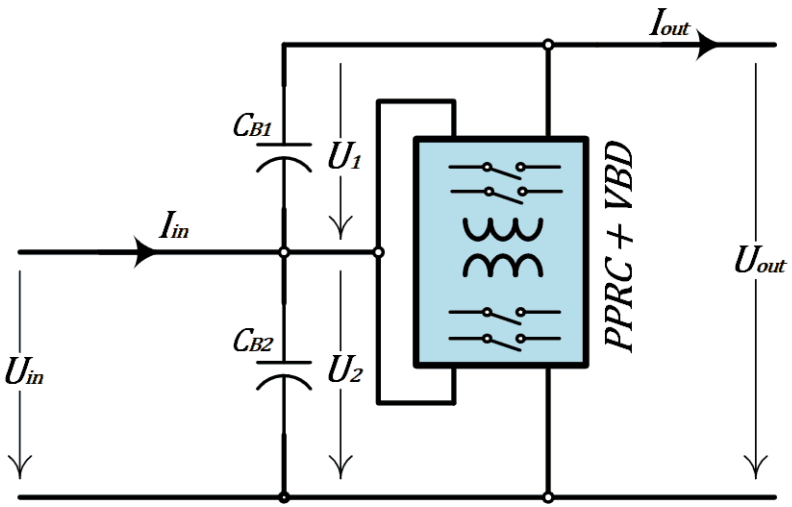
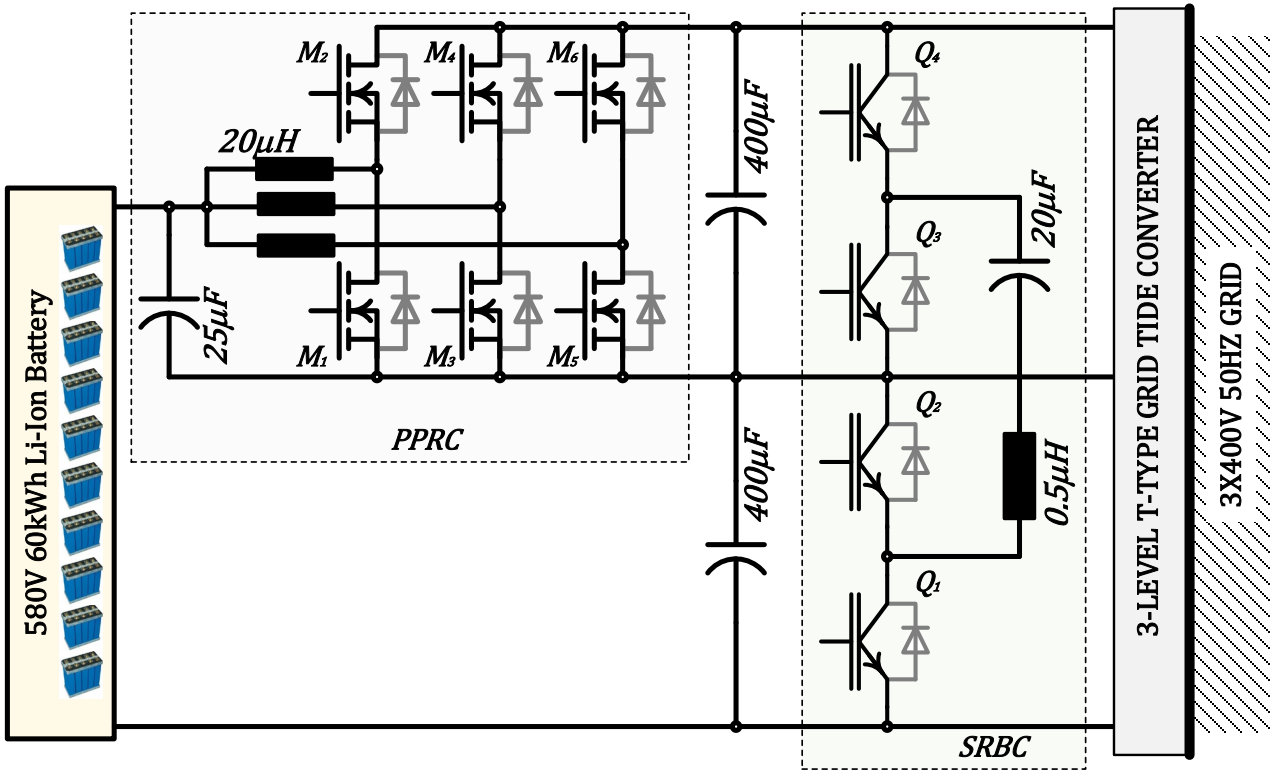


- Similar concept can be used with TOP Input-BOTTOM Output ISO VBD
  - U_1 to U_2 voltage ratio is not constant
  - $U_{out} > U_{in}$ (BOOST)
  - The converter is PPRC + VBD
    - DAB
    - SRC
    - LLC
    - PS FB

Case 1: Battery Interface DC-DC Converter

Interface DC-DC converter for grid connected Li-Ion battery energy storage system

- $U_{B(n)} = 580\ [V]$
- $U_{B(min)} = 460[V]$
- $U_{B(max)} = 660V[V]$
- $U_{BUS} = 700\ [V]$
- $P_{B(n)} = 30[kW]$
- $f_{sw(PPRC)} = 100\ [kHz]$
- $f_{sw(SR-VBD)} \cong 50\ [kHz]$
- SR-VBD
  - IGBT IKW75N65EL5
- PPRC:
  - CoolMOS IPZ60R017C7



❖ P. J. Grbović, "Partial Power Rated DC/DC Converters: A Way to Go Beyond the Limits"
- 30kW
- >99.5% Efficiency…>50kW/dm³ & 25kW/kg….Si Only (no WBG)!!

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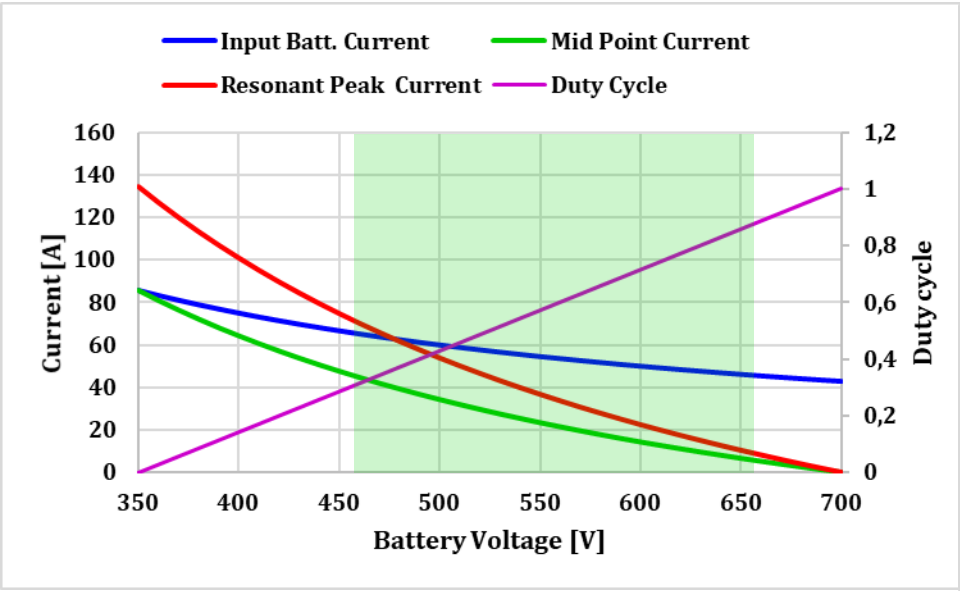

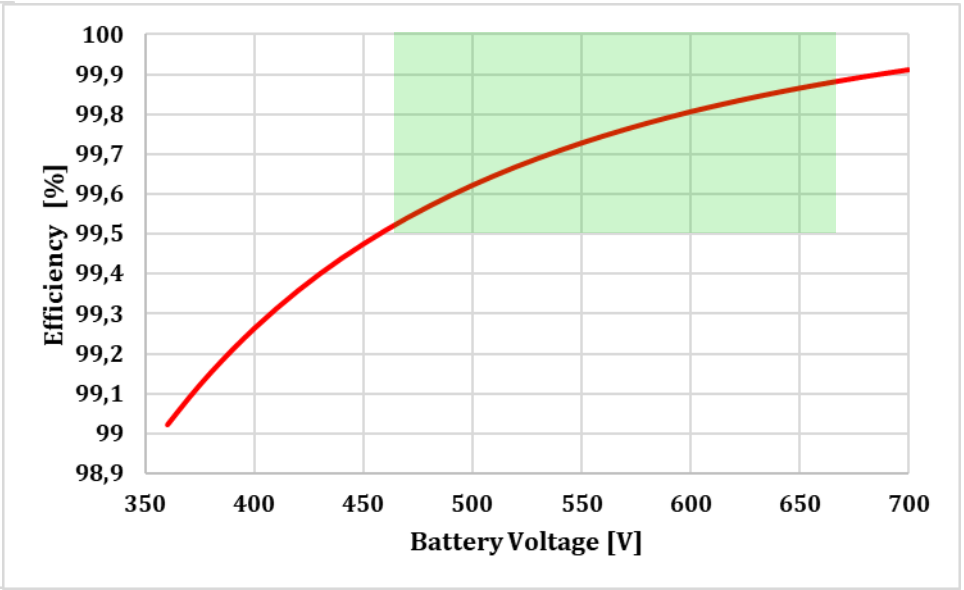

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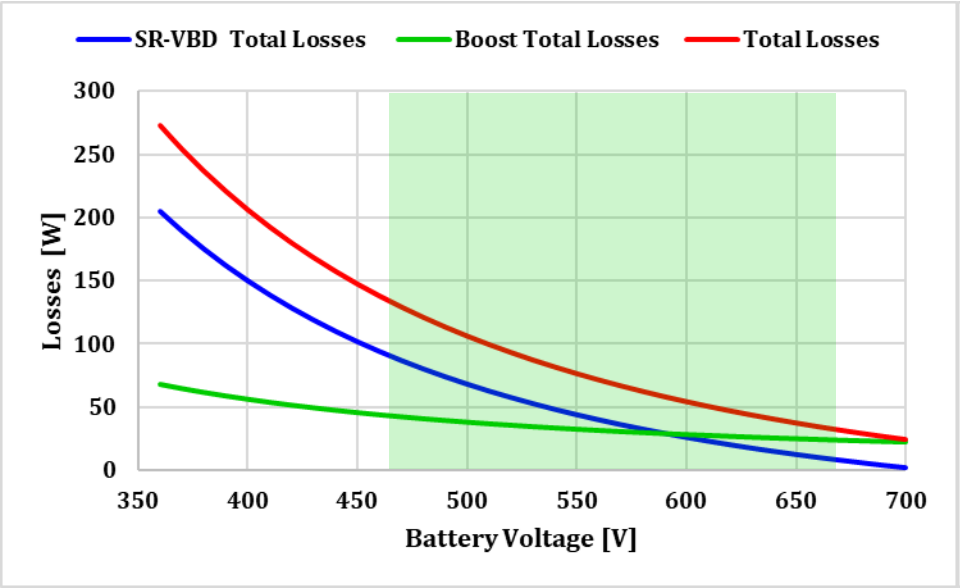

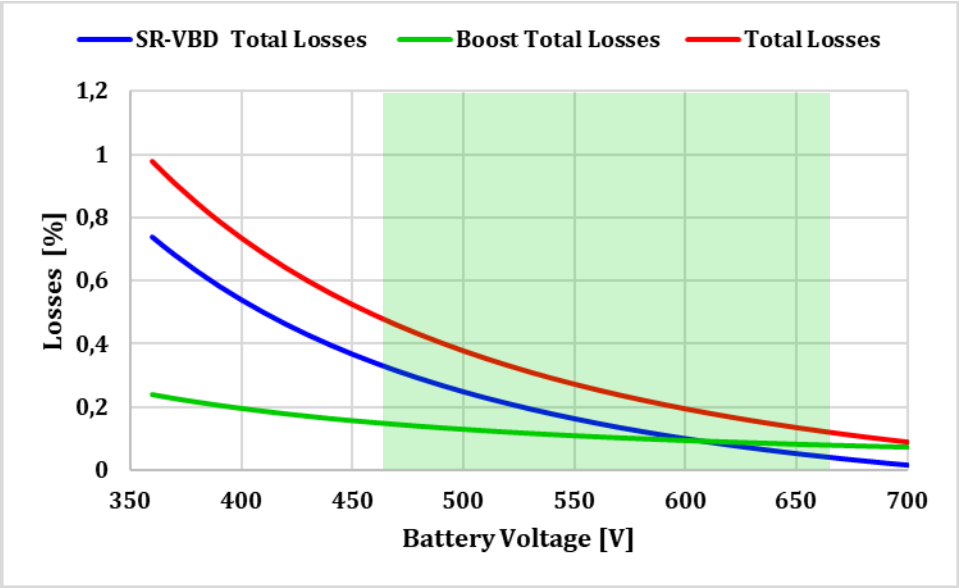

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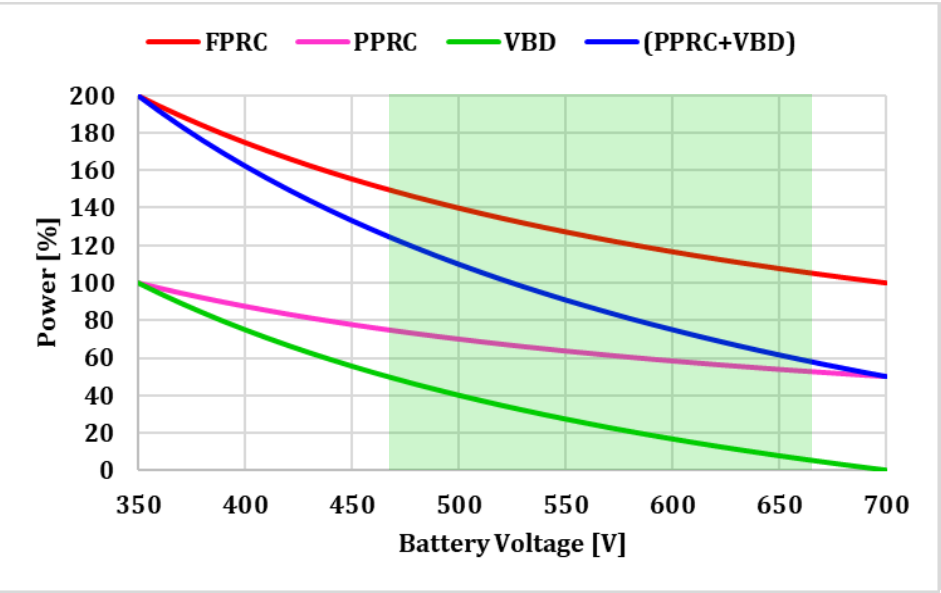
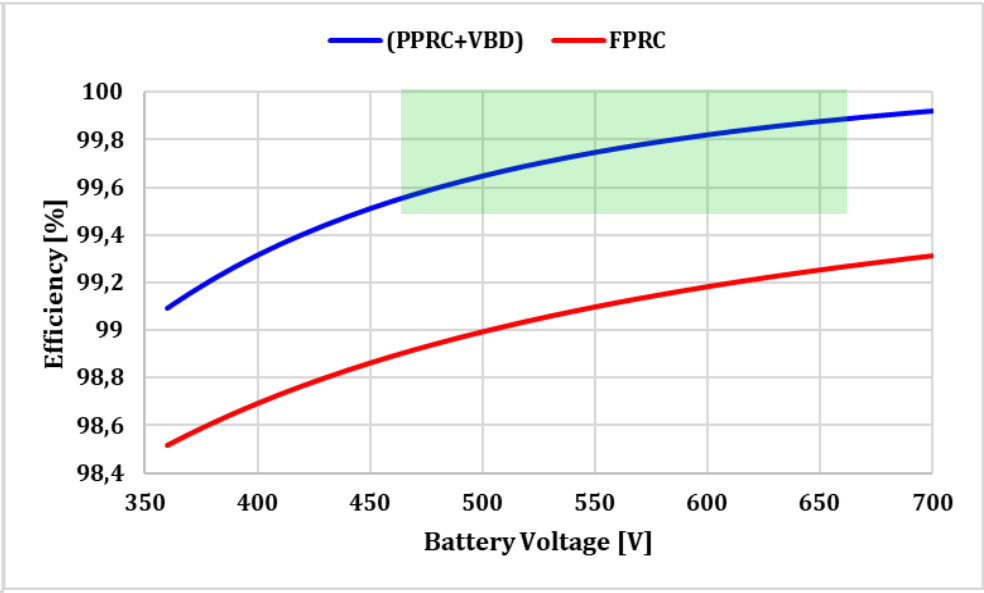




PPRC+SR-VBD

- $f_{sw(PPRC)} = 100\ [kHz]$
- $f_{sw(SR-VBD)} \cong 50\ [kHz]$
- SR-VBD (IGBT IKW75N65EL5)
- PPRC (3 x CoolMOS IPZ60R017C7)
- $L_{out} = 20[\mu H]\ C_{out} = 25[\mu F]$ @ 450V

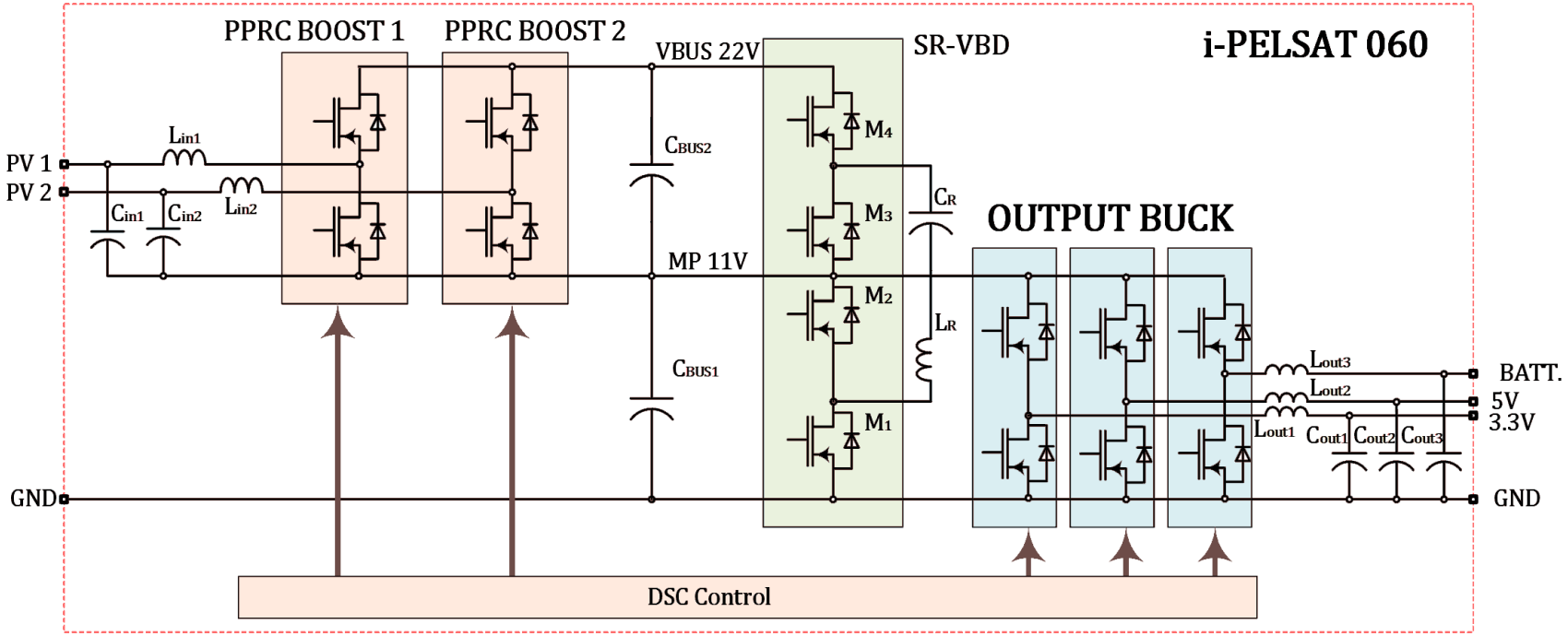
FPRC

- $f_{sw(FPRC)} = 15\ [kHz]$
- IGBT FPRC (FP40R12KT3)
- $L_{out} = 200[\mu H]$
- $C_{out} = 180[\mu F]$ @ 900V

Case 2: Nano-Satelit Power Supply

- Power Supply for Nano Satellite
- Input 2 x PV Panels (20Vmax & 3Amax)
- Storage Battery (8V 2600 mAh)

- Outputs:
  - 5V @ 4A
  - 3,3 V @ 5A



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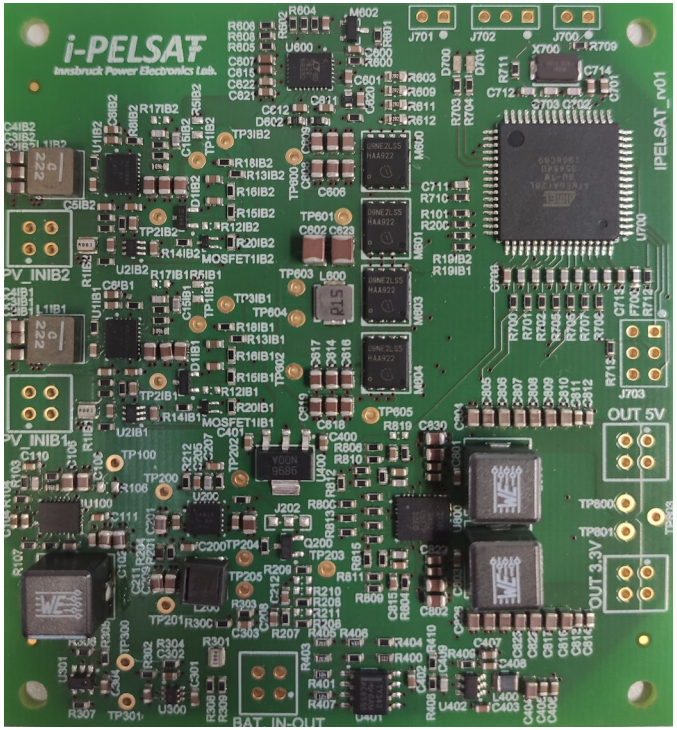

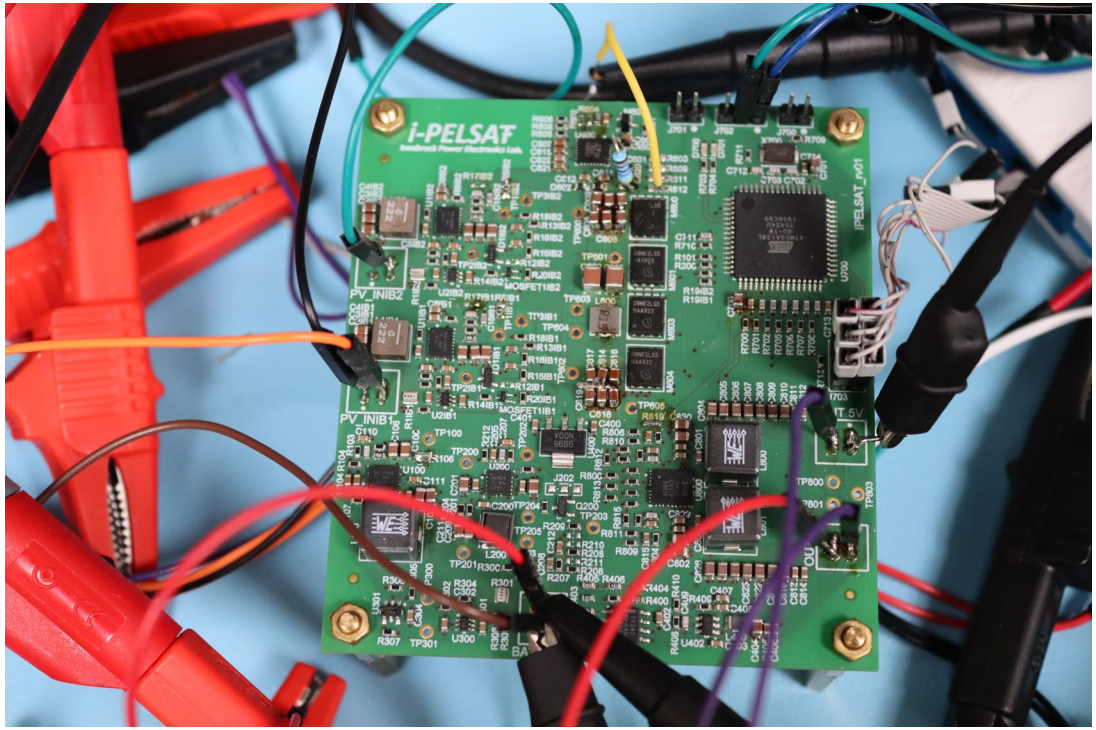

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SPECIFICATION	UNIT	TARGET	PROTORYPE	COMPARISON
Maximum power consumption	[W]	5	5,5	111 [%]
Maximum PCB weight	[g]	200	34	17 [%]
Maximum dimension (L x W x H)	[mm]	90x96x25	78x87x8,7	27 [%]
Maximum voltage ripple@ 5V, 4A	[mV]	100	18	18 [%]
Maximum current ripple@ 5V, 4A	[mA]	120	12	10 [%]
Maximum voltage ripple@ 3,3V, 5A	[mV]	66	14	21 [%]
Maximum current ripple@ 3,3V, 5A	[mA]	150	12	8 [%]

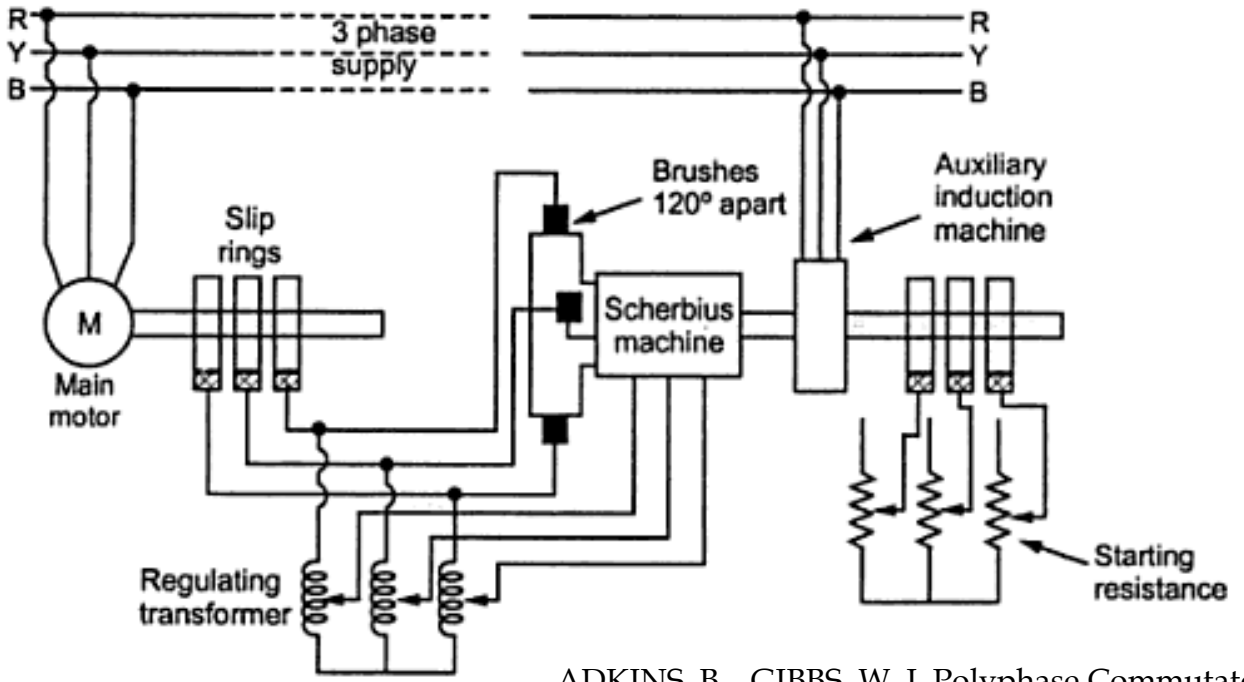
Partial Power Rated Converters

Is the PPRC a new concept?

Partial Power Rated Converters

Is the PPRC a new concept?

- In fact not very new...
  - Slip Power Recovery or Scherbius Drive

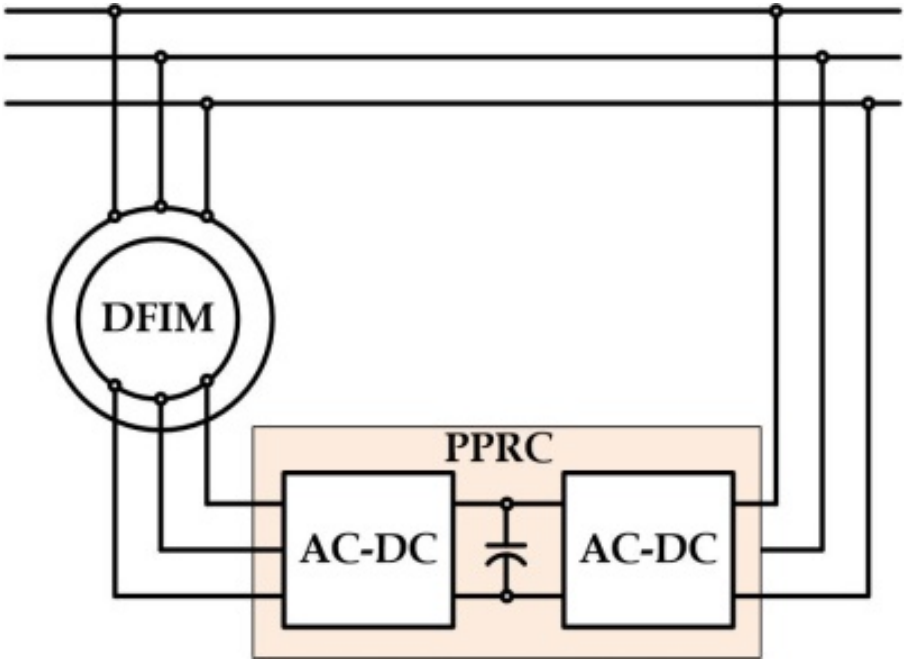


ADKINS, B. , GIBBS, W. J. Polyphase Commutator Machines. 1951

Partial Power Rated Converters

Is the PPRC a new concept?

- In fact not very new...
  - Slip Power Recovery or Scherbius Drive
  - Double Fed Induction Machine



We need to explore existing topologies and use them in different way

a) Partial Power Processing Converters

b) **Current Source Converters**

c) Multi-Cell & Multi-Level Converters

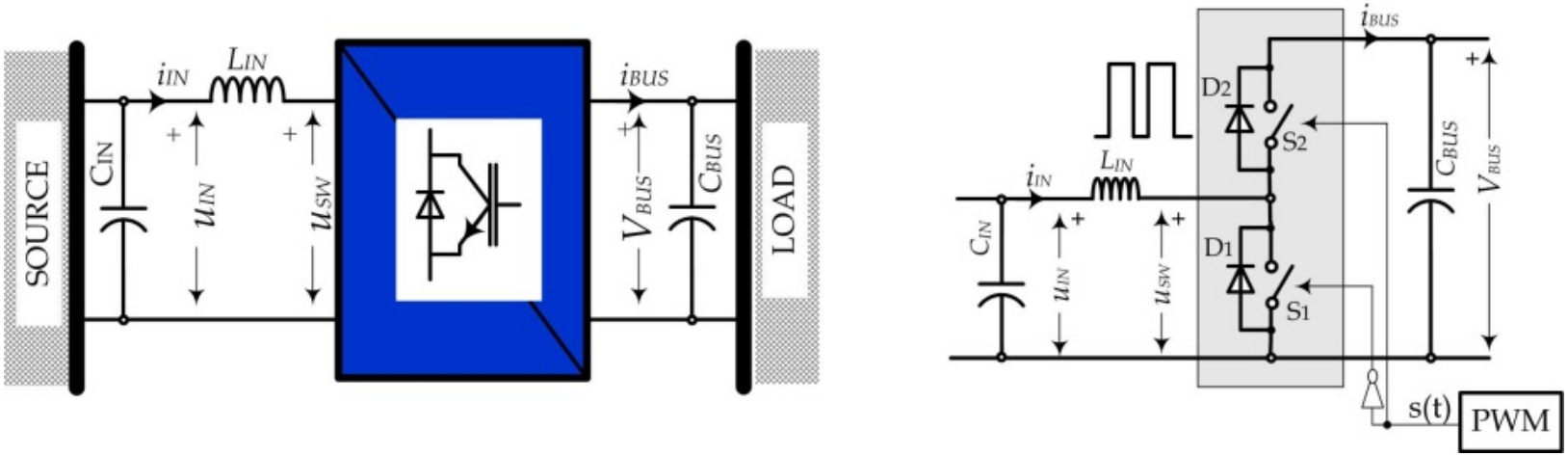
d) Quantum Mode Resonant Converters

Current Source Converters

-Switch the current instead of voltage-

Current Source Converters

- Theory of Duality
  - Voltage ↔ Current, Inductor ↔ Capacitor, Node ↔ loop, Series ↔ parallel
- PWM Voltage Source ↔ Current Source Converter



Voltage Source Converter VSC

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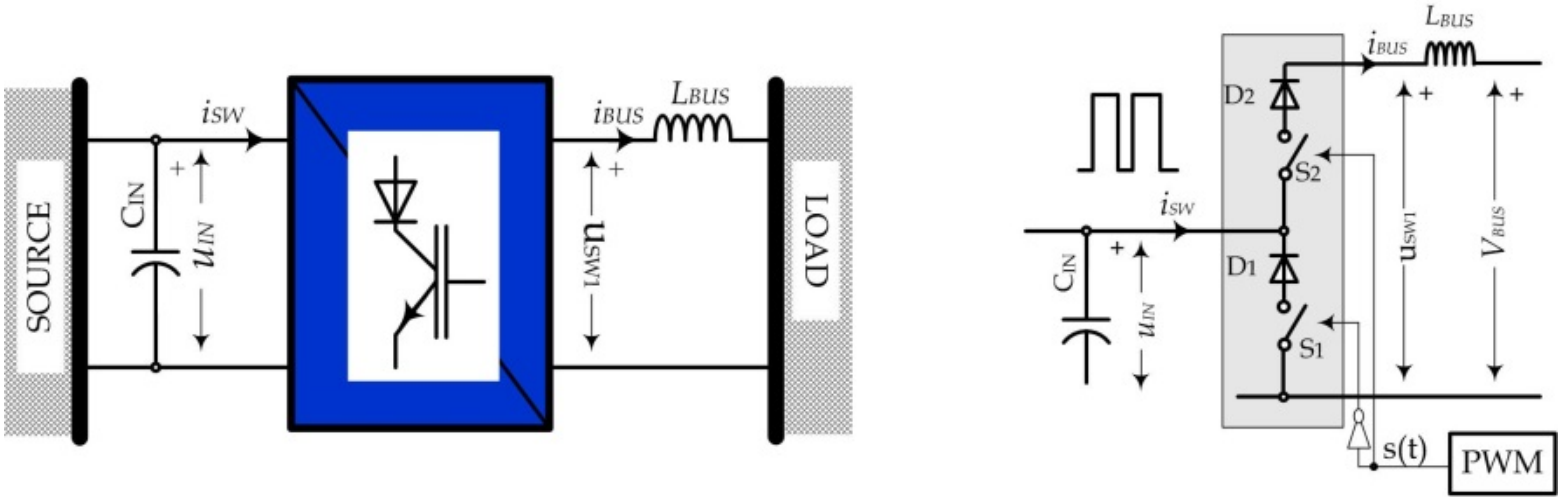
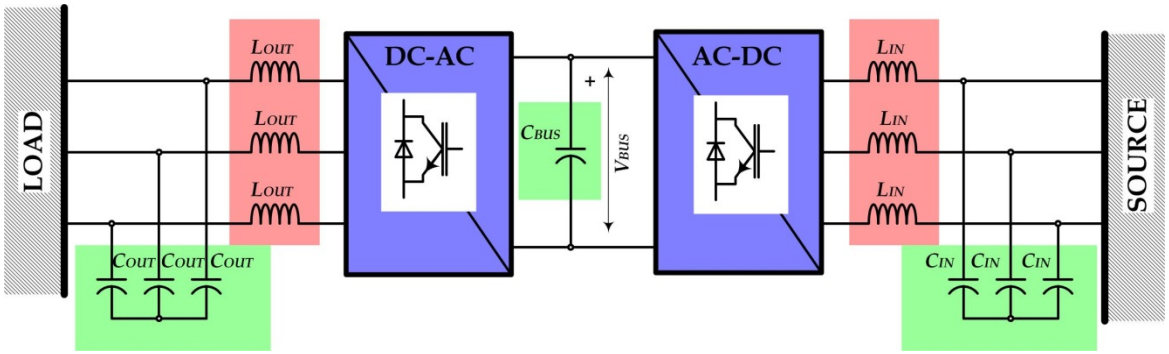


Current Source Converter CSC

Current Source Converters

- 3 Phase PWM VSC
  - 1 dc bus capacitor
  - 6 big filter Inductors
  - 6 Filter capacitors



- 3 Phase PWM CSC
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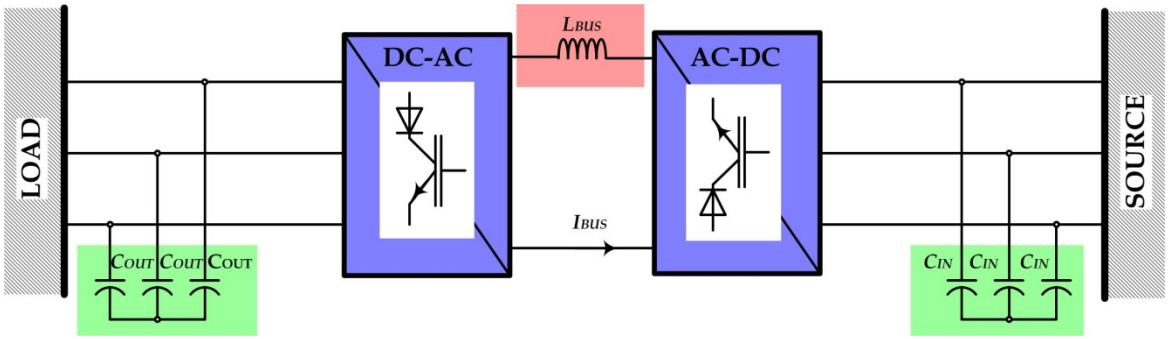
  - 6 big filter Caps.

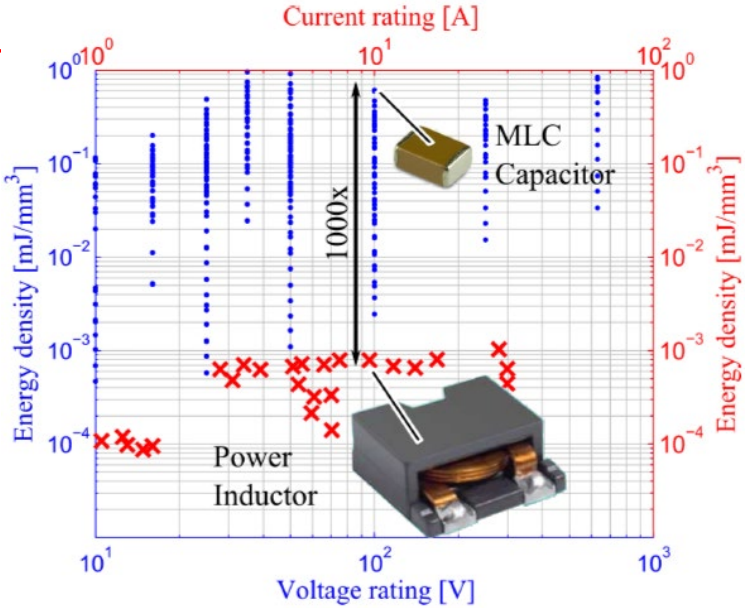


- Is there any difference between VSC & CSC?

Current Source Converters

- Is there any difference between VSC & CSC?
- Energy Density of Capacitors and Inductors
  - Film Caps. W_C=40-80 [J/kg]
  - **MLCC much better**
  - MF Inductors W_L=0.2-1 [J/kg]

The CSC should be better than the VSC?



Robert Pilawa-Podgurski, "High density capacitor-based power converters - application challenges and requirements" March 3rd, 2018PSMA/PELS Capacitor Workshop

Current Source Converters

- It looks like CS Converters have bright future?

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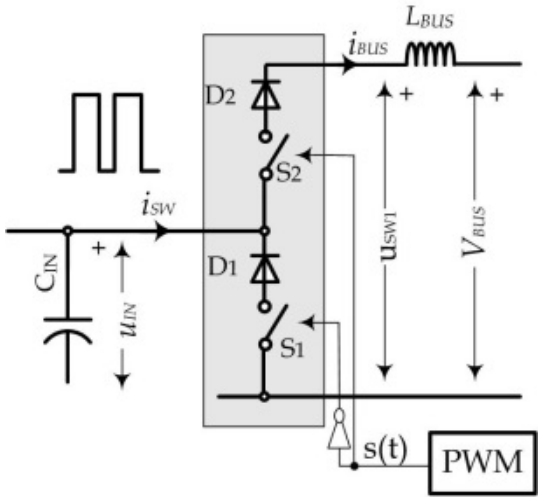
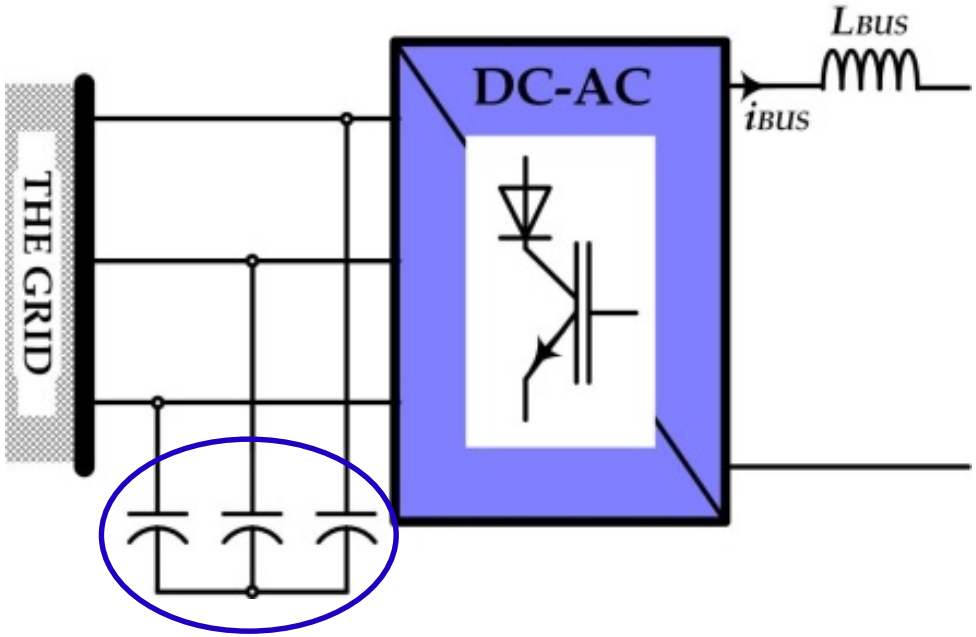
  - Yes But, "No meal for free"



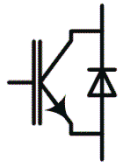


Grid Filter caps C_{IN} are stressed with high current pulses !!

⇒ Relatively big caps....⇒ The Grid is not very happy !!

Current Source Converters

- It looks like CS Converters have bright future?
  - Yes But, "No meal for free"
- Existing power semiconductors are perfectly matched with PWM VSCs
  - Current bi-directional Switch…MOSFETs, IGBTs+FWD….



- PWM CSCs require different switch
  - Voltage Bi-directional Switch, but high frequency

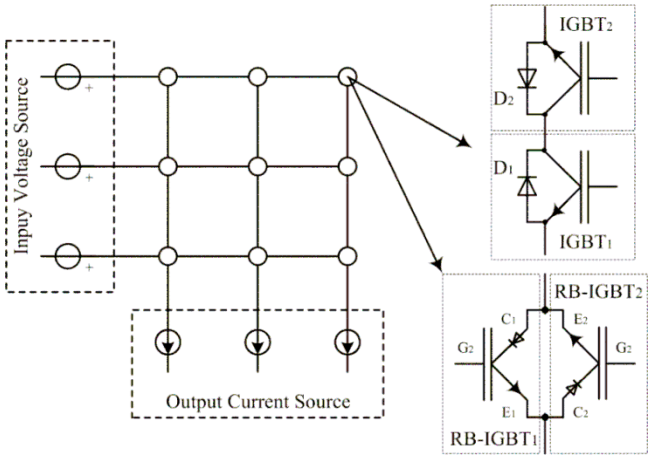
- This should be focus for future research

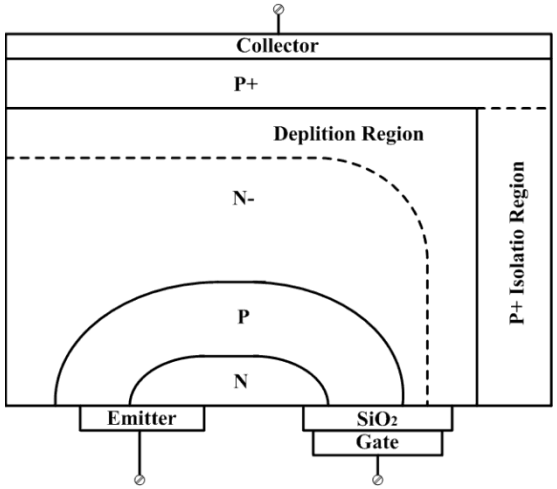
Current Source Converters

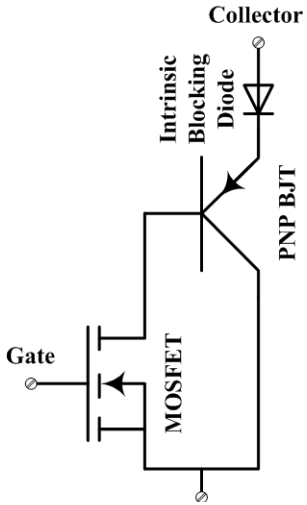
Reverse Blocking IGBT

- An IGBT is naturally reverse blocking device, but….
- Not required in most of applications
  - Minimized to optimize the switching performances
  - Typically 10-50V
- Matrix and current source converters requires full RB capability

- Additional p+ layer provides full RB capability
  - An "intrinsic" blocking diode
- Better conduction performances, but worst switching (turn-off)
  - Preferred solution in low frequency range <10kHz
- The same dynamic modal as an ordinary IGBT







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b) Current Source Converters

c) **Multi-Cell** & Multi-Level Converters

d) Quantum Mode Resonant Converters

Multi-Cell Interleaved Converters

-Split the (inductor) load current into segments-

Multi-cell Converters

Why we need to split the load (output) current into segments?

I. Good topic for (university) research,
II. Can we do something for passives (Inductors & Capacitors)?
III. Something else?
IV. And, is it a logical step?

Multi-cell Converters

High power (and/or high performances) converters

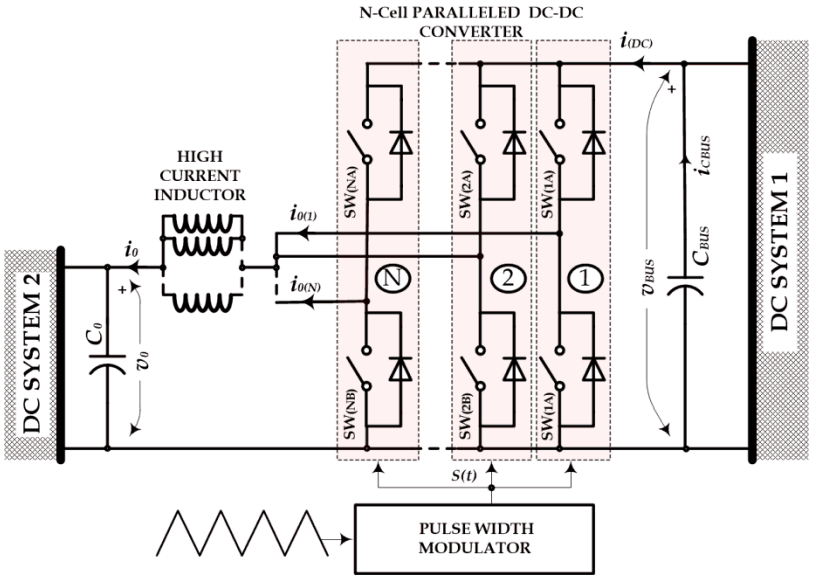
- **Paralleling of power semiconductors is a need**

High power (and/or high performances) converters

- ❑ **Paralleling of power semiconductors is a need**

1. Direct Paralleling

- ❑ Easy control, but
- ❑ The current sharing is an issues..
- ❑ No additional benefits



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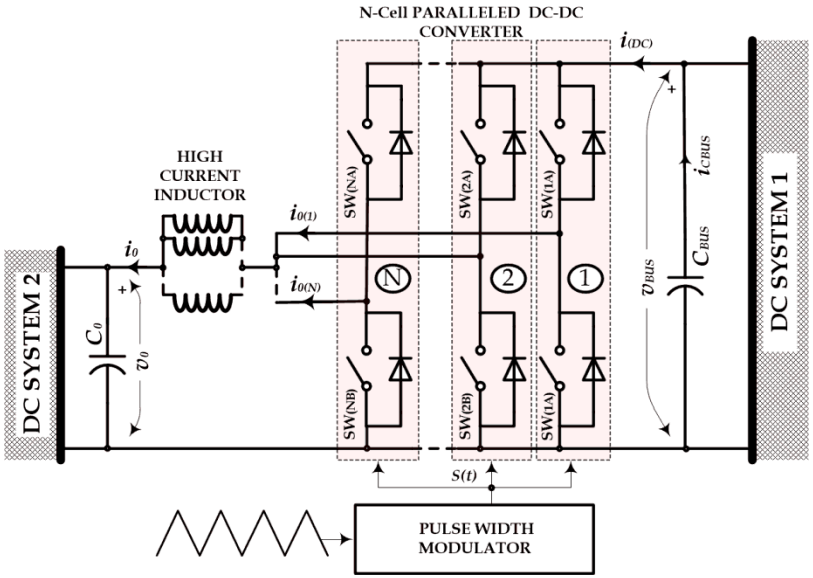
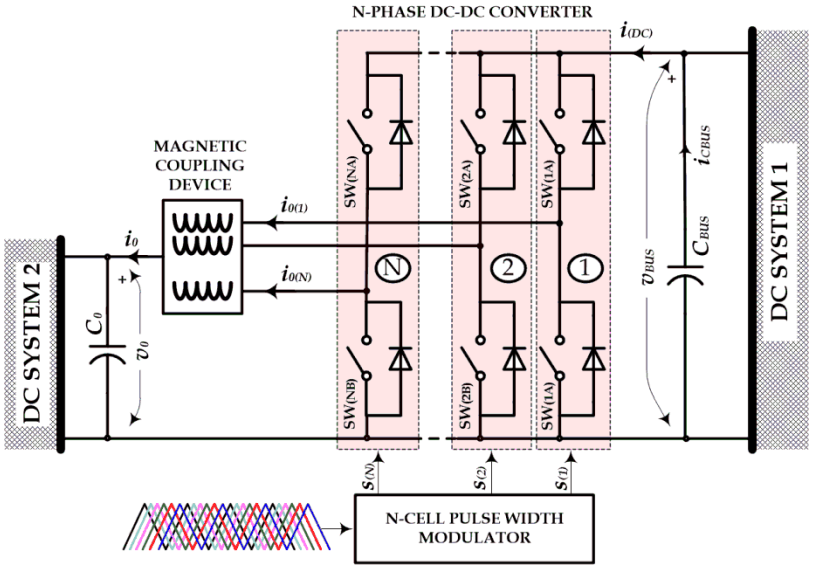


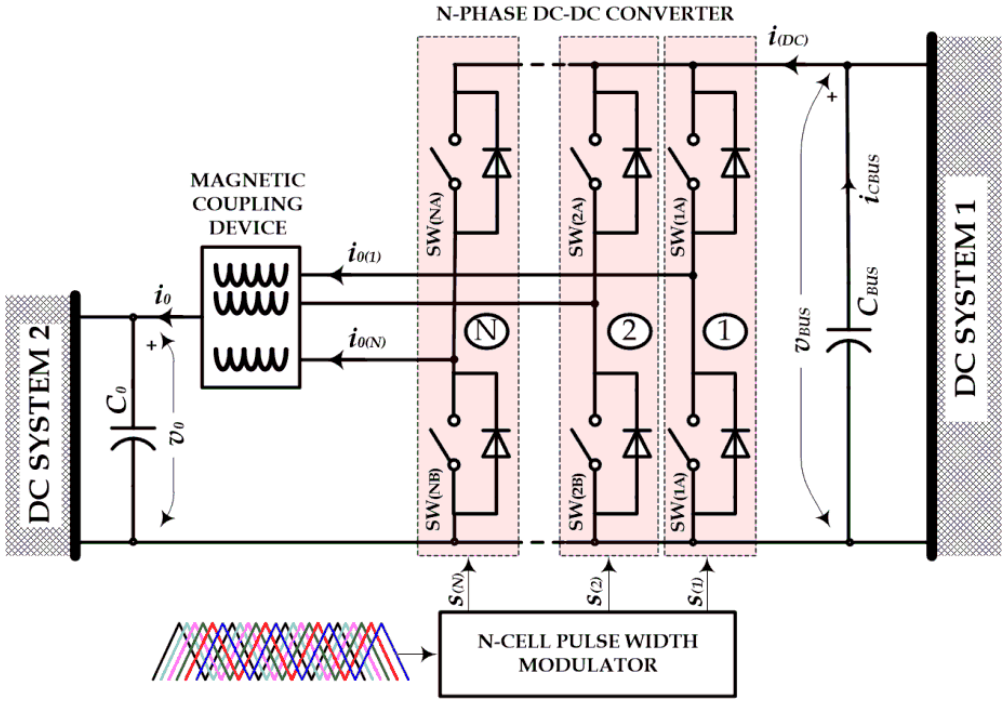
2. Paralleling with Interleaving

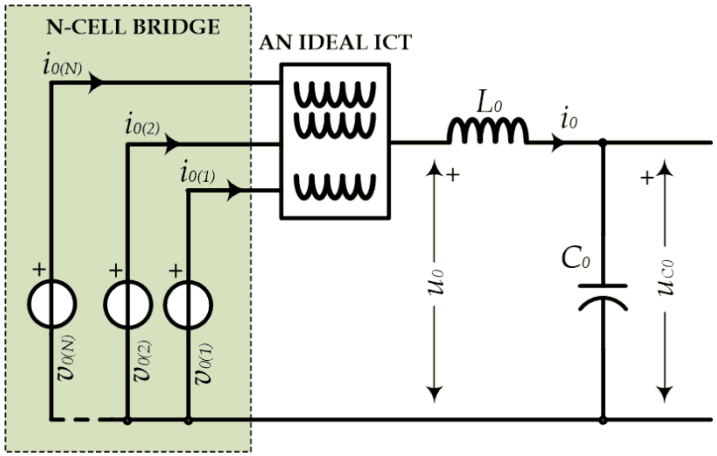
- ❑ More expensive, but
- ❑ Better performances (filter size/cost, losses, control…)



Multi-cell Converters

- Intelligent paralleling of devices
- **I**ndividual, **I**ntelligent & **I**nterleaved **C**ontrol -IIIC

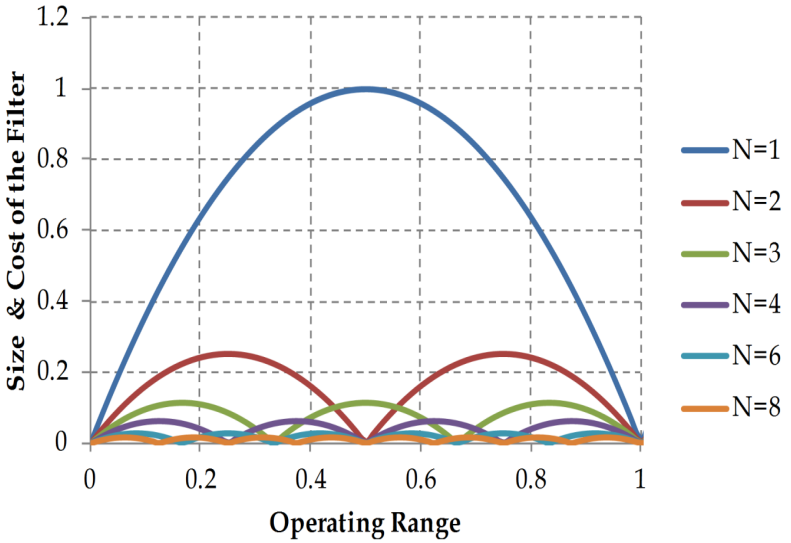


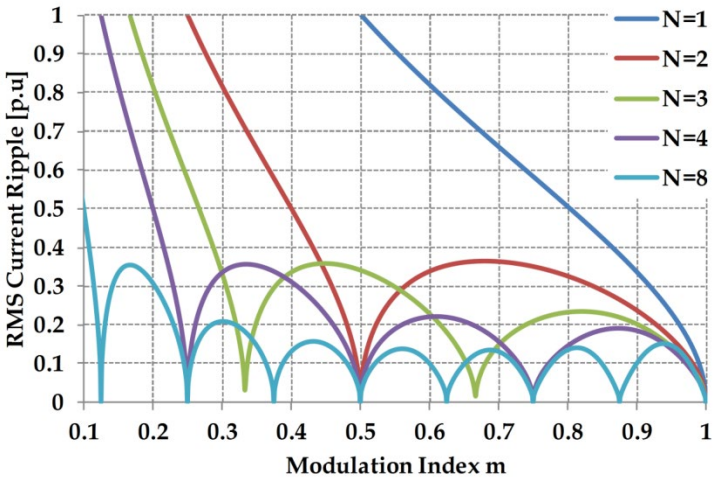


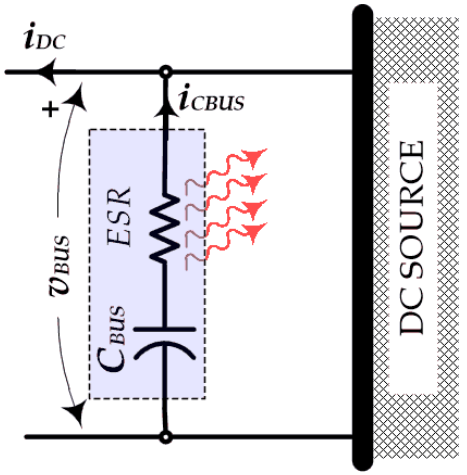
Multi-cell Converters

Harmonics Cancelation

- The input filter cost and size
- The DC Bus Current and DC Bus capacitor stress and losses

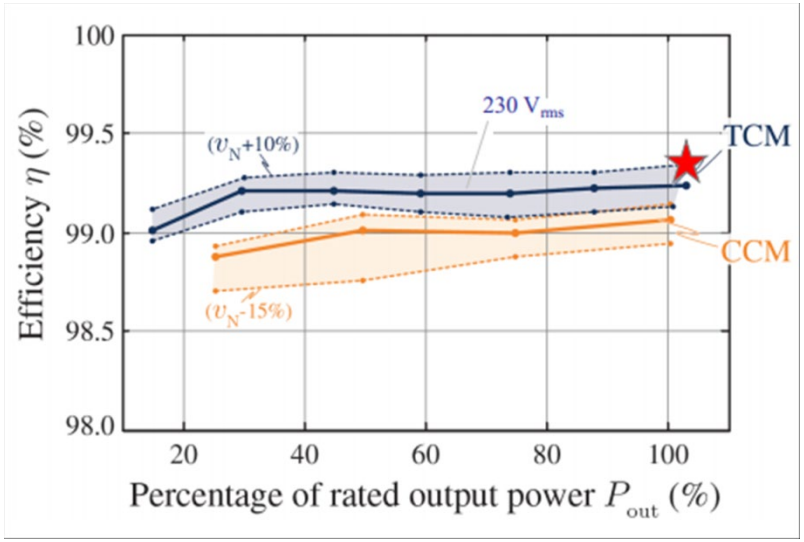


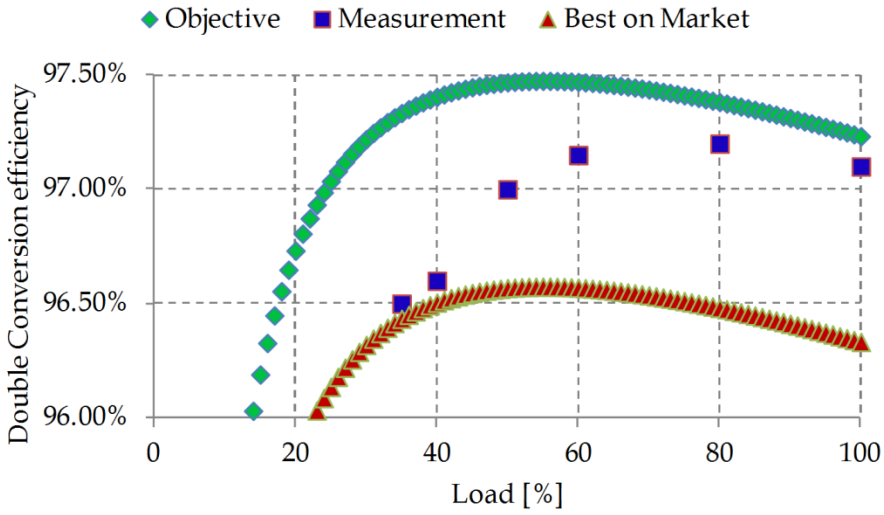




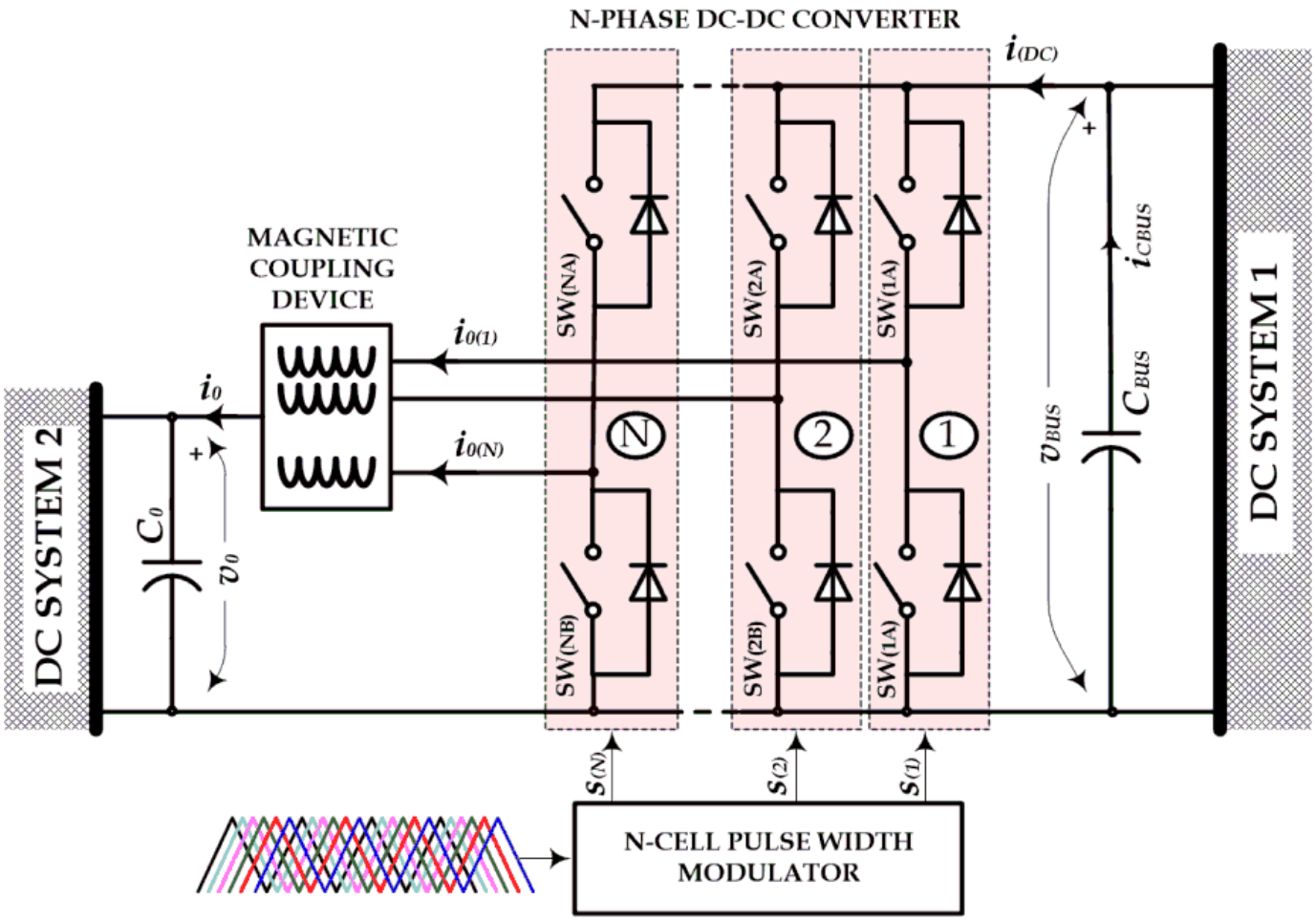
Multi-cell Converters

- 99.3% efficient single phase PFC/Inverter..
  - ETH /Professor J.W. Kolar
- 97.8 % efficient double conversion 100kVA/3U UPS
  - ECCE Huawei Technologies
- All this would not be possible without Interleaving



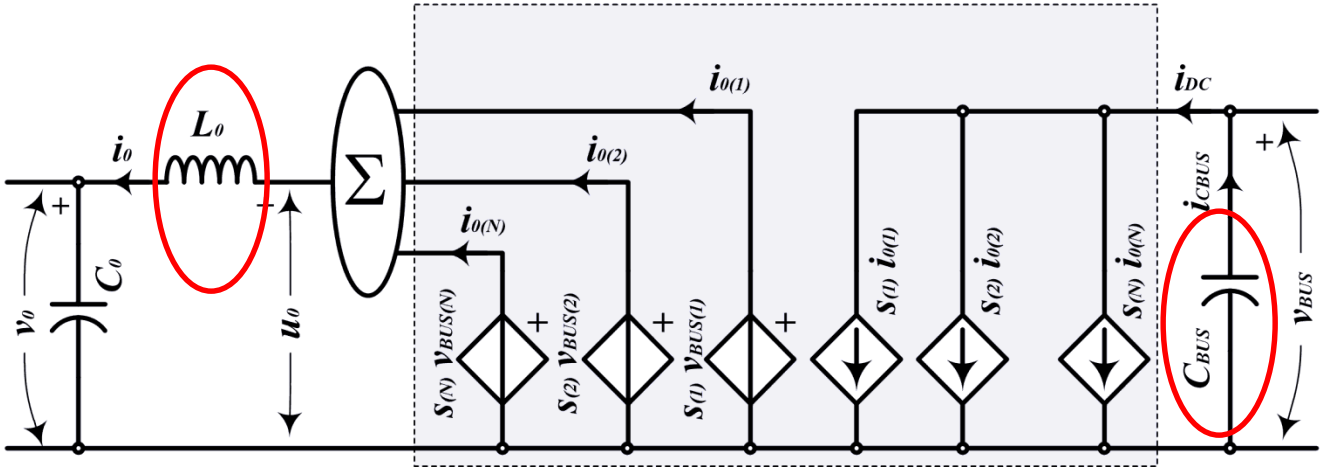


Multi-cell Converters



N-cell Converter Analysis

- In General, How does it Work?



- k^{th} cell switching function

$$s_{(k)}(t) = d + \frac{2}{\pi}\sum_{p=1}^{\infty}\frac{1}{p}\sin(pd\pi)\cos\left(p\omega_{SW}t + \frac{2\pi}{N}(k-1)\right) \qquad k = (1,2,\ldots N)$$

- Output voltage u_0 and dc bus current i_{DC}

$$v_0(t) = \sum_{k=1}^{N}\frac{v_{0(k)}(t)}{N} = \frac{V_{BUS}}{N}\sum_{k=1}^{N}s_k(t) \qquad i_{DC}(t) = \sum_{k=1}^{N}s_{(k)}(t)\,i_{0(k)}(t)$$

N-cell Converter Analysis

- N-Cell Converter output voltage u_0

1
$$u_0(t) = dV_{BUS} + V_{BUS}\frac{2}{\pi}\sum_{p=1}^{\infty}\left[\frac{1}{p}\sin(pd\pi)\sum_{k=1}^{N}\cos\left(p\omega_{SW}t + \frac{2\pi}{N}(k-1)\right)\right]$$

2a
$$\cos(\alpha+\beta) = \cos(\alpha)\cos(\beta) - \sin(\alpha)\sin(\beta)$$

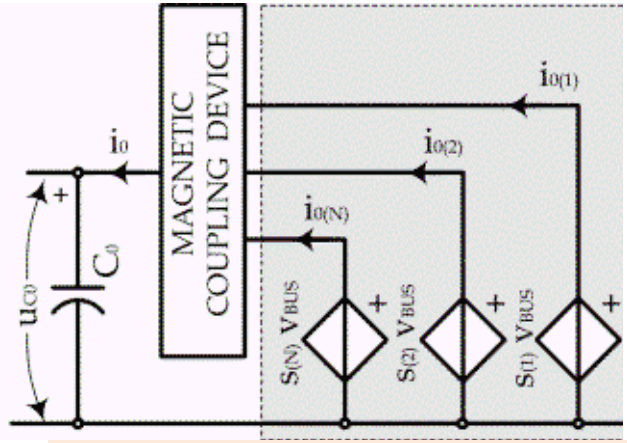
2b
$$\sum_{k=1}^{N}\cos p\frac{2\pi}{N}(k-1) = \begin{cases} 1 & p = iN \\ 0 & p \neq iN \end{cases} \quad i = \{1..\infty\}$$

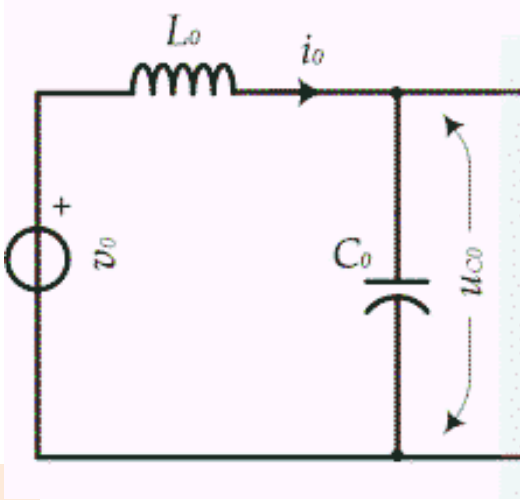
2c
$$\sum_{k=1}^{N}\sin p\frac{2\pi}{N}(k-1) = 0$$

- All harmonics up to N^{th} are canceled from the output voltage

3
$$u_0(t) = dV_{BUS} + \frac{V_{BUS}}{N}\frac{2}{\pi}\sum_{i=1}^{\infty}\left[\frac{1}{i}\sin(iNd\pi)\cos(iN\omega_{SW}t)\right]$$

N-cell Converter Analysis





$$L_0 \frac{di_0}{dt} = v_0(t) - u_{C0}$$

$$\Delta i_0(t) = \frac{\Delta i_0(d)}{2} \begin{cases} -1 + N \dfrac{\Delta i_0(d)}{dT_{sw}} t & 0 \le t \le d\dfrac{T_{sw}}{N} \\ 1 - N \dfrac{\Delta i_0(d)}{(1-d)T_{sw}} \left(t - d\dfrac{T_{sw}}{N} \right) & d\dfrac{T_{sw}}{N} \le t \le \dfrac{T_{sw}}{N} \end{cases}$$

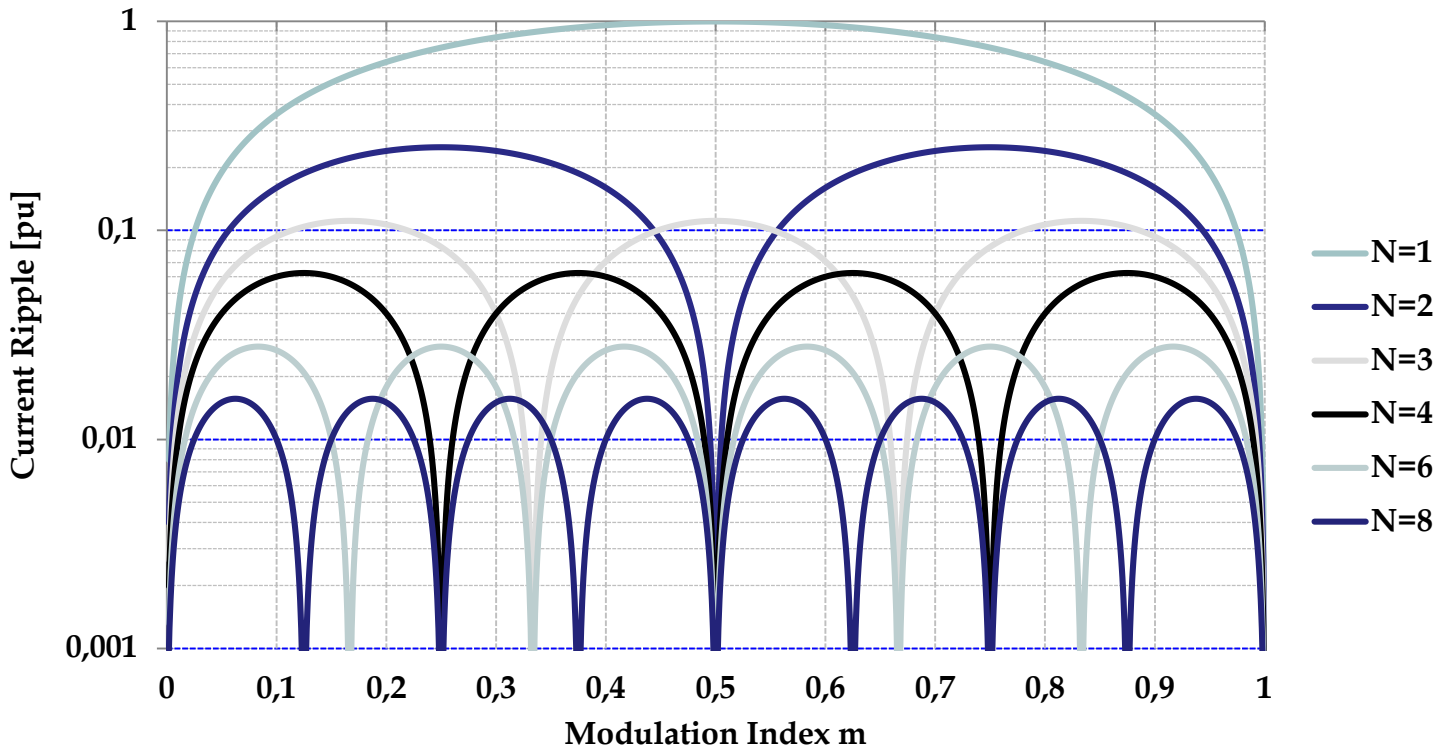
- The Inductor Current Ripple

$$\Delta i_0(d) = \left(\frac{V_{BUS}}{4 f_{SW} L_0} \right) \frac{4}{N^2} \left[(Nd - floor(Nd)) - (Nd - floor(Nd))^2 \right] = \left(\frac{V_{BUS}}{4 f_{SW} L_0} \right) K_{\Delta i}(d)$$

N-cell Converter Analysis

- The Inductor Current Ripple…..

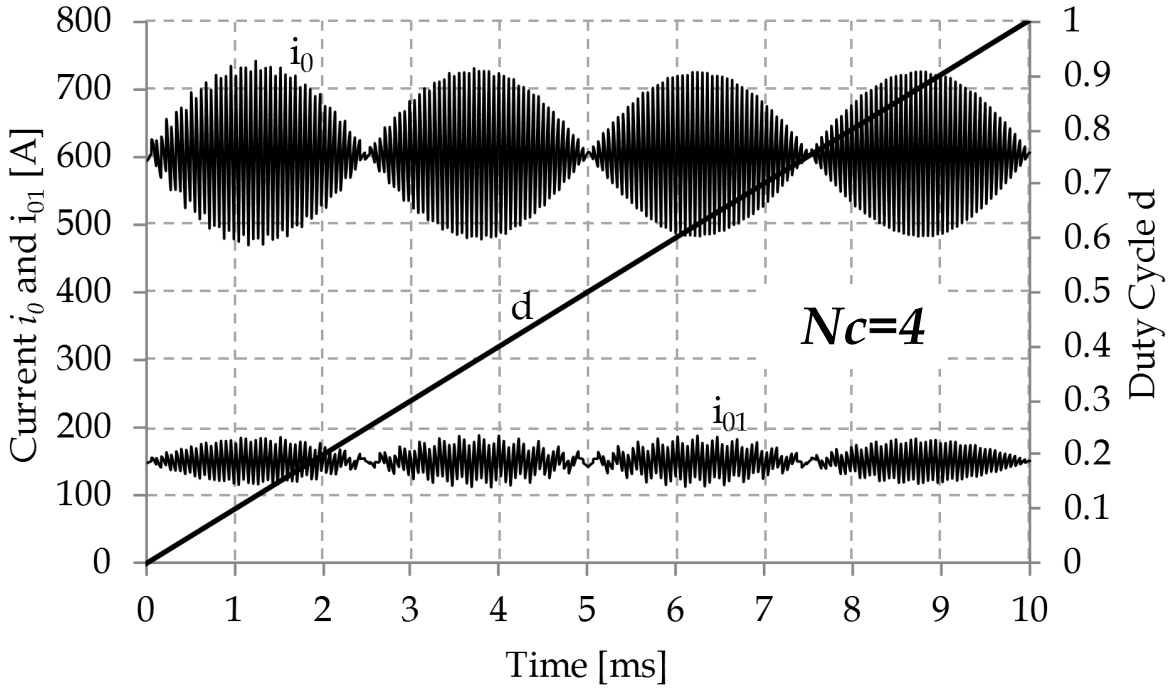
$$\Delta i_0(d) = \left(\frac{V_{BUS}}{4 f_{SW} L_0}\right)\frac{4}{N^2}\left[(Nd - floor(Nd)) - (Nd - floor(Nd))^2\right] = \left(\frac{V_{BUS}}{4 f_{SW} L_0}\right) K_{\Delta i}(d)$$



N-cell Converter Analysis

- The Inductor Current Ripple…..

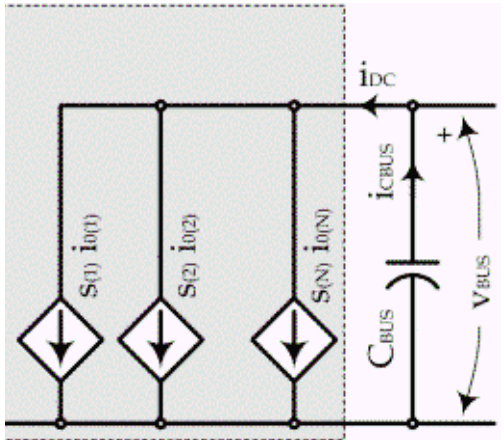
$$\Delta i_0(d) = \left(\frac{V_{BUS}}{4 f_{SW} L_0}\right) \frac{4}{N^2} \left[(Nd - floor(Nd)) - (Nd - floor(Nd))^2 \right] = \left(\frac{V_{BUS}}{4 f_{SW} L_0}\right) K_{\Delta i}(d)$$

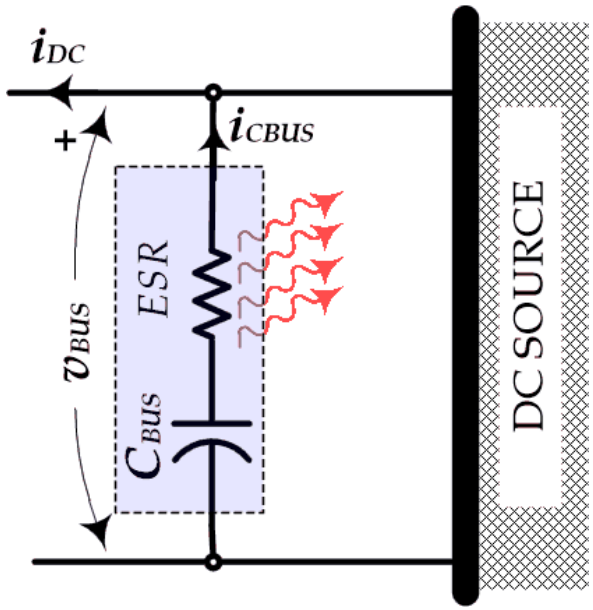


N-cell Converter Analysis

DC Bus Current i_{DC}

- Capacitor stress
- Losses
- Voltage Ripple
- **The Cap. Size/cost**





$$i_{DC}(t) = \sum_{k=1}^{N} s_{(k)}(t) i_{OUT(k)}(t)$$

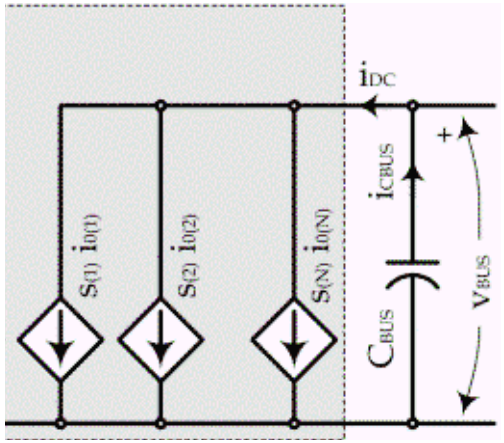
$$i_{(DC)}(t) = \sum_{k=1}^{N} d_{(k)} I_{0(k)} + \sum_{k=1}^{N} I_{0(k)} \frac{2}{\pi} \sum_{p=1}^{\infty} \frac{1}{p} \sin(pd\pi) \cos\left(p\omega_{SW} t + \frac{2\pi}{N}(k-1) \right) + \sum_{k=1}^{N} d_{(k)} \Delta i_{0(k)}(t)$$

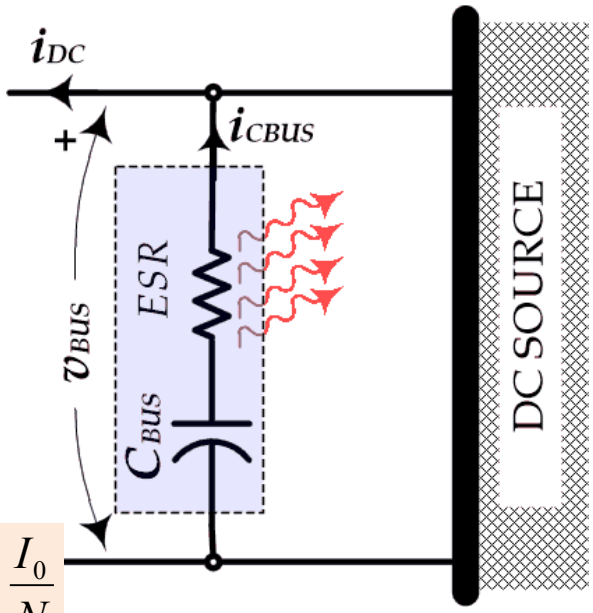
$$+ \underbrace{\sum_{k=1}^{N} \Delta i_{0(k)}(t) \frac{2}{\pi} \sum_{p=1}^{\infty} \frac{1}{p} \sin(pd\pi) \cos\left(p\omega_{SW} t + \frac{2\pi}{N}(k-1) \right)}_{\cong 0}$$

N-cell Converter Analysis

DC Bus Current i_{DC}

- Capacitor stress
- Losses
- Voltage Ripple
- **The Cap. Size/cost**





$$i_{DC}(t) = \sum_{k=1}^{N} s_{(k)}(t) i_{OUT(k)}(t)$$

$$d_{(1)} = \ldots = d_{(N)} = d \;\&\; I_{0(1)} = .. = I_{0(N)} = \frac{I_0}{N}$$

$$\Delta i_{0(1)}(t) = \Delta i_{0(2)} = .. = \Delta i_{0(N)}(t) = \frac{\Delta i_0(t)}{N}$$

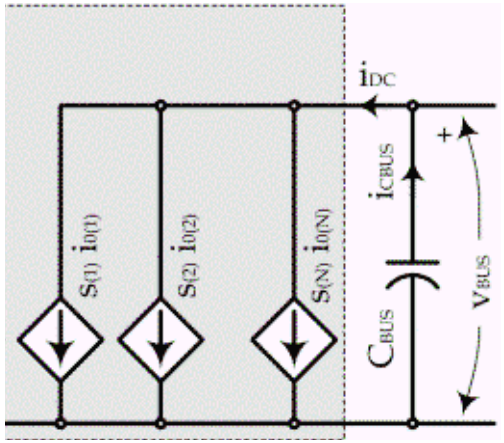
$$i_{(DC)}(t) \cong dI_0 + I_0 \frac{2}{\pi} \sum_{p=1}^{\infty} \left[\frac{1}{p} \sin(pd\pi) \sum_{k=1}^{N} \cos\left(p\omega_{SW} t + \frac{2\pi}{N}(k-1) \right) \right] + d\Delta i_0(t)$$

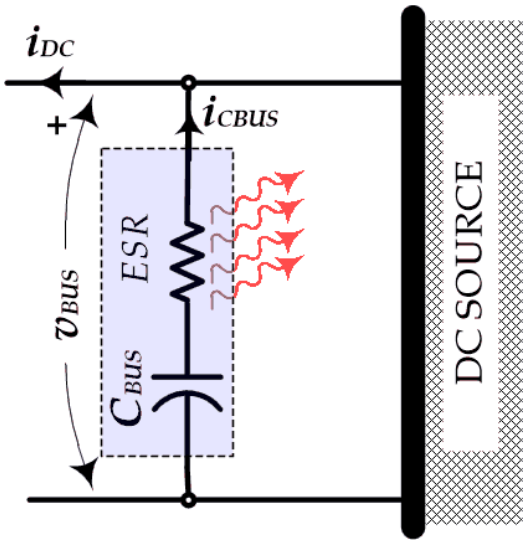
$$= dI_0 + \underbrace{\frac{I_0}{N} \frac{2}{\pi} \sum_{i=1}^{\infty} \left[\frac{1}{i} \sin(iNd\pi) \cos(iN\omega_{SW} t) \right]}_{i_{CBUS}(t)} + d\Delta i_0(t)$$

N-cell Converter Analysis

DC Bus Current i_{DC}

- Capacitor stress
- Losses
- Voltage Ripple
- **The Cap. Size/cost**





RMS Current

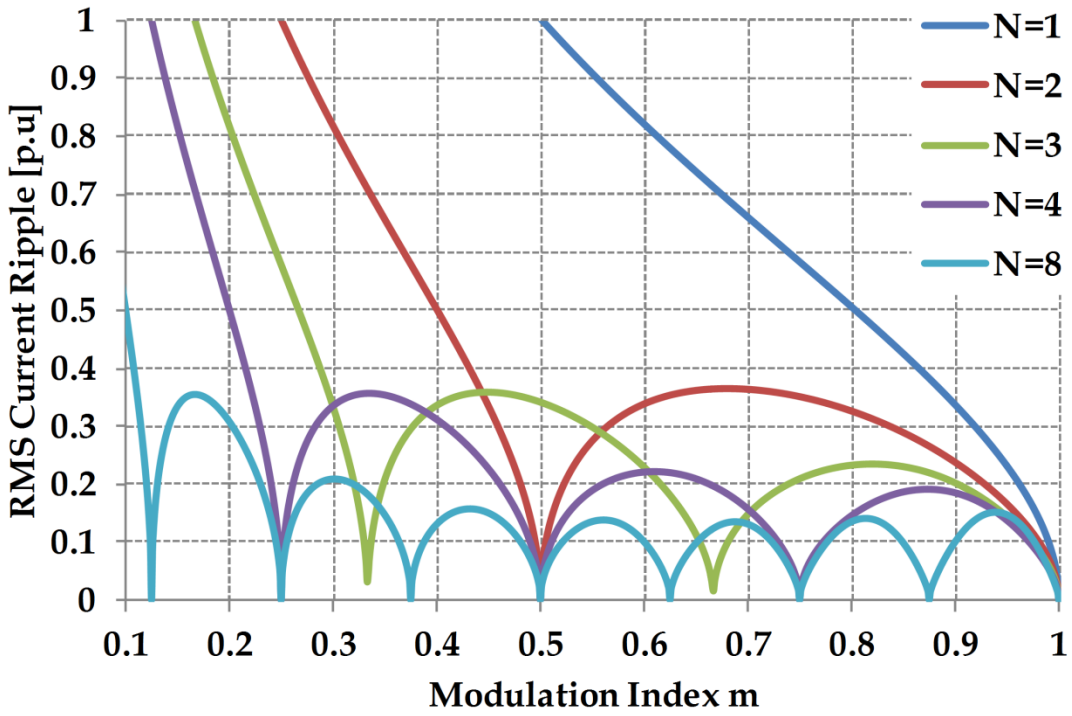
$$I_{CBUS(RMS)} = \sqrt{\frac{1}{T}\int_0^T i_1^2(t)dt + \frac{1}{T}\int_0^T i_2^2(t)dt + \underbrace{\frac{1}{T}\int_0^T i_1 i_2(t)dt}_{=0}} = \sqrt{\left(\frac{I_0}{N}\frac{\sqrt{2}}{\pi}\right)^2 \sum_{i=1}^{\infty}\frac{1}{i^2}\sin^2(iNd\pi) + d^2\Delta i_{0(RMS)}^2}$$

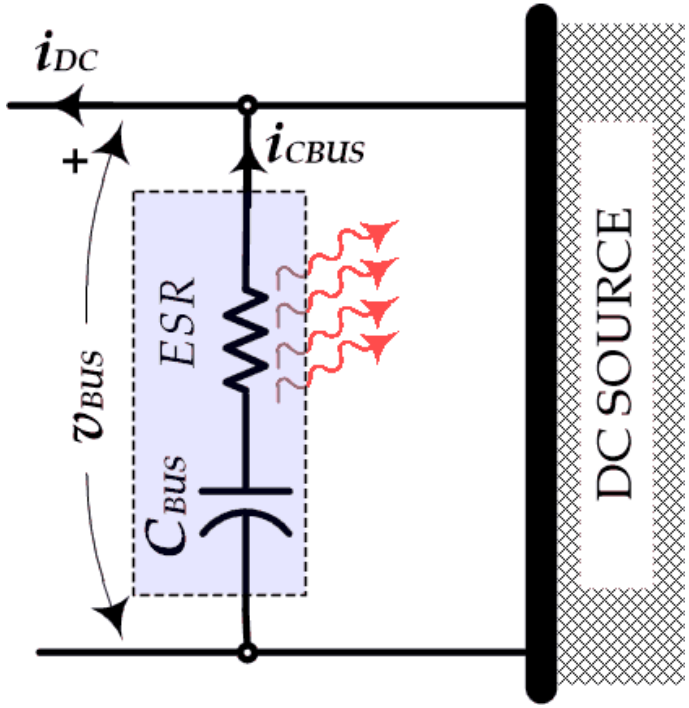
Petar J. Grbović, "Closed Form Analysis of N-Cell Interleaved Two-Level DC-DC Converters: The DC Bus Capacitor Current Stress Analysis," ECCE Asia 2013, Down Under, IEEE Energy Conversion Congress and Exposition, Melbourne, Australia, 3-6 June, 2013.

N-cell Converter Analysis

RMS Current

$$I_{CBUS(RMS)} = \frac{P_{C0}}{V_{BUS}} \sqrt{\frac{\left[(Nm - floor(Nm)) - (Nm - floor(Nm))^2\right]}{(Nm)^2} + \left(\frac{V_{BUS}}{P_{C0}} \Delta i_{0(\max)} m \frac{2}{\sqrt{3}}\right)^2 \left[(Nm - floor(Nm)) - (Nm - floor(Nm))^2\right]^2}$$





N-cell Converter Analysis

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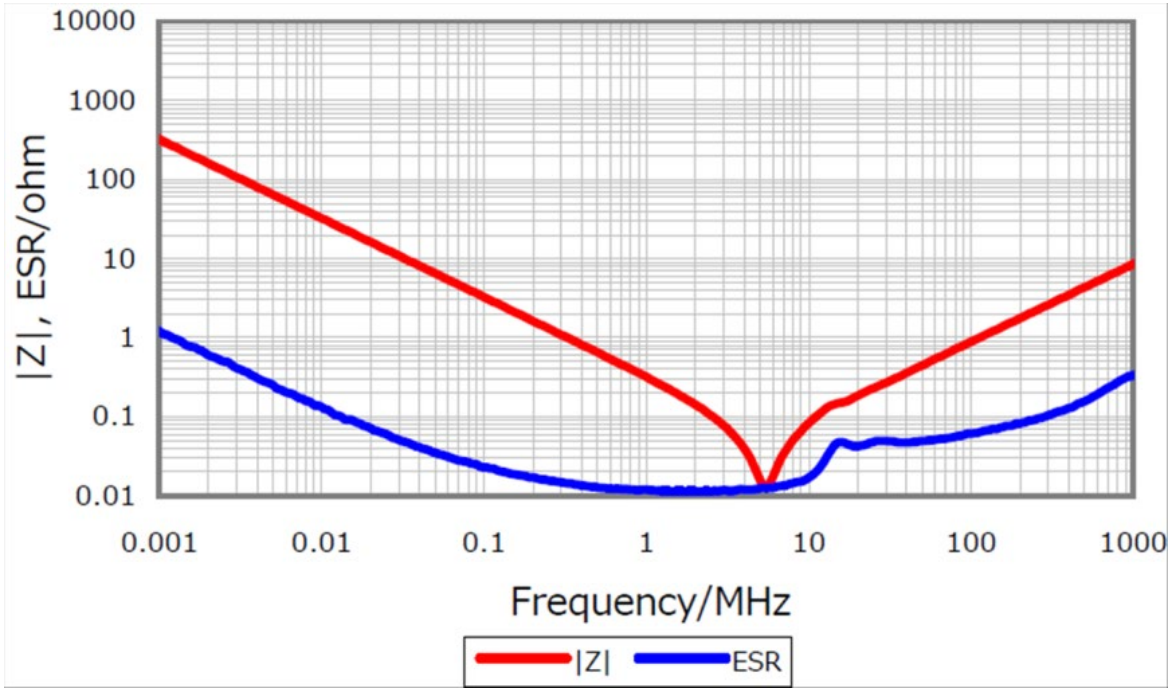
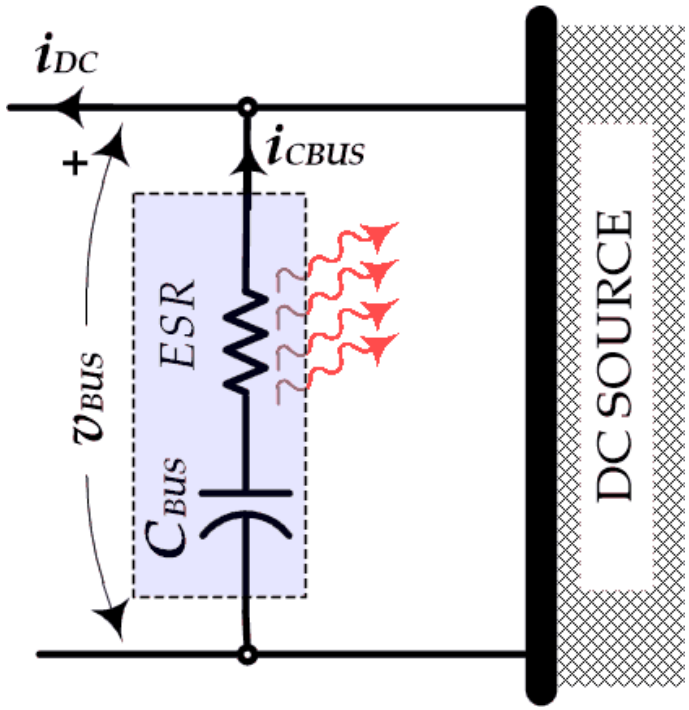


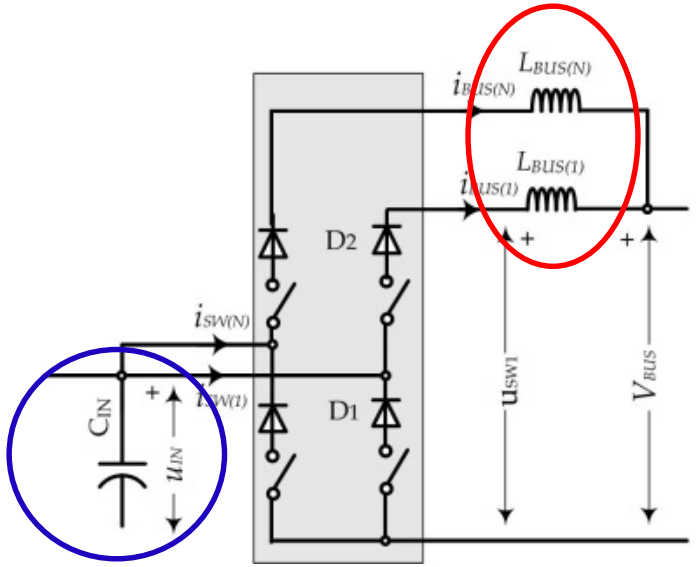
MLCC

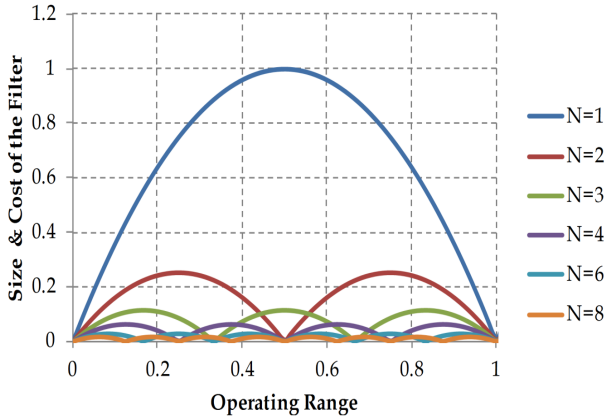


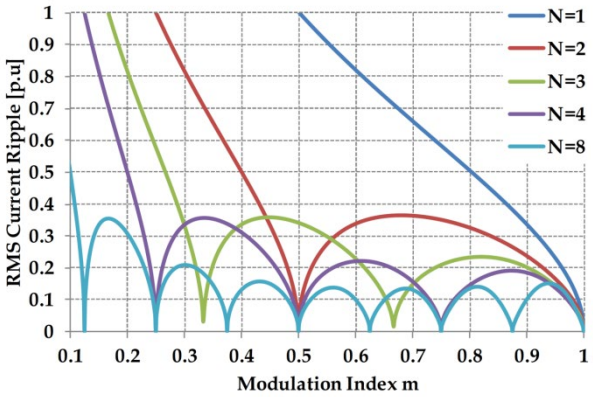
N-cell CSC

Go back to CSC

- **Input Capacitor & Current Stress!!**
- **N-Cell Interleaved CSC**
  - **Small Grid Side Filter Capacitor…**
  - **Small DC Bus Inductors**







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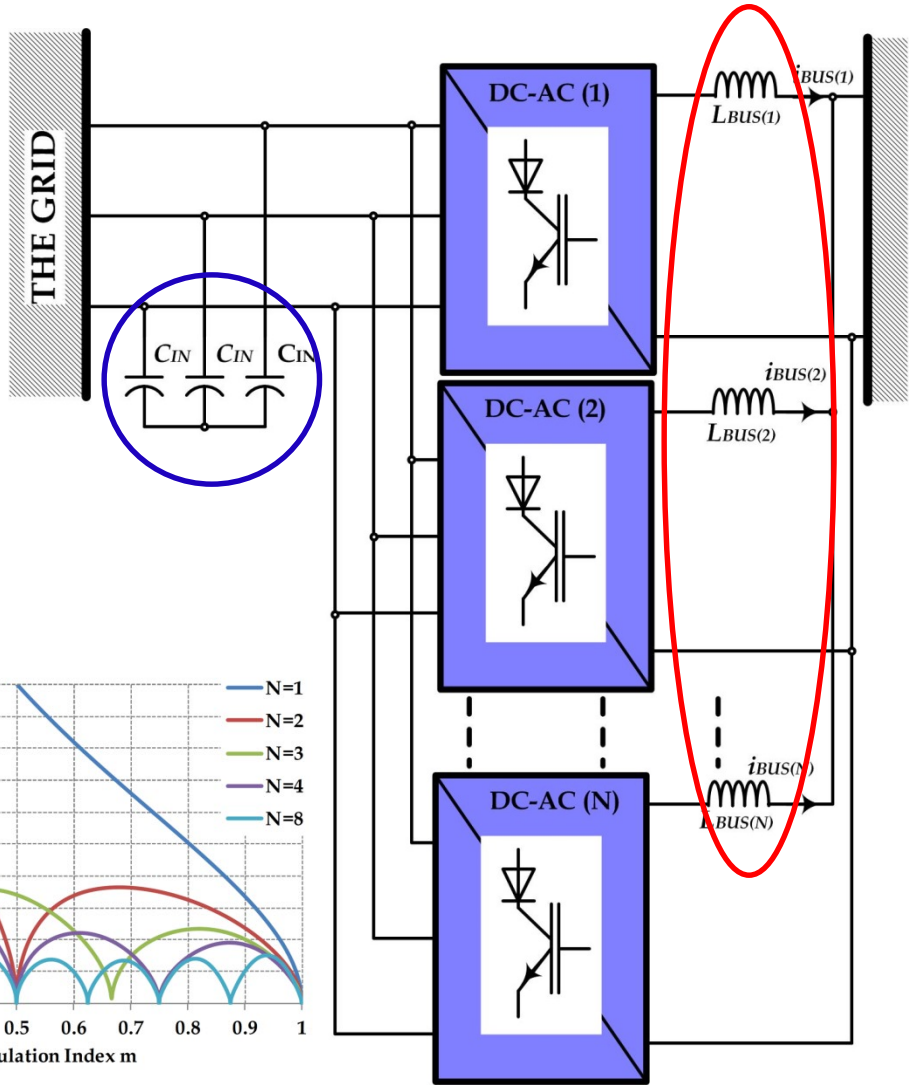
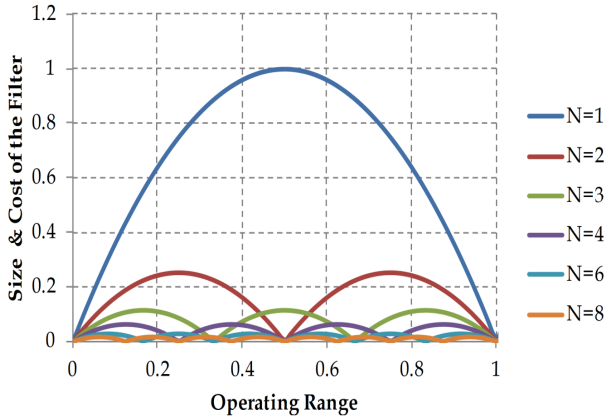
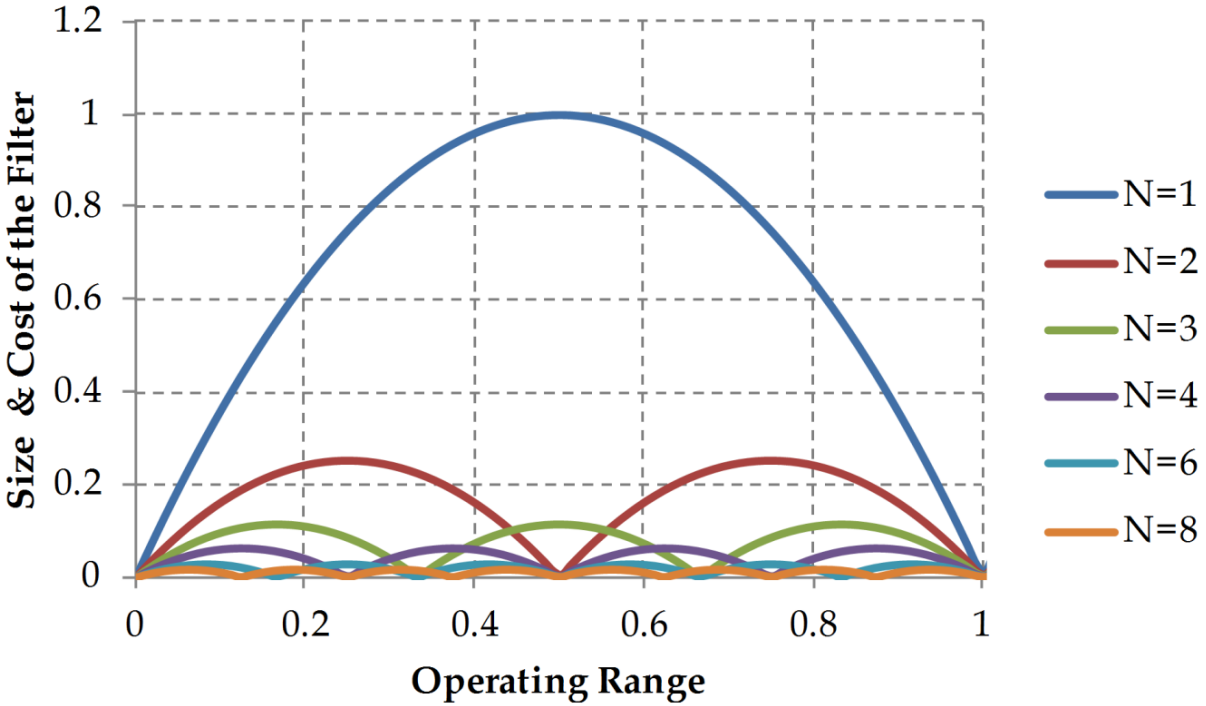




Multi-cell Converters

Interleaving ➡ Filter cost/size reduction



What ELSE?

Interleaving ⇒ Filter cost/size reduction

What ELSE?

I. Reduced equivalent stray inductance of the switching cell, or

II. Reduced equivalent switching speed of a device

⇒ Higher switching speed is possible

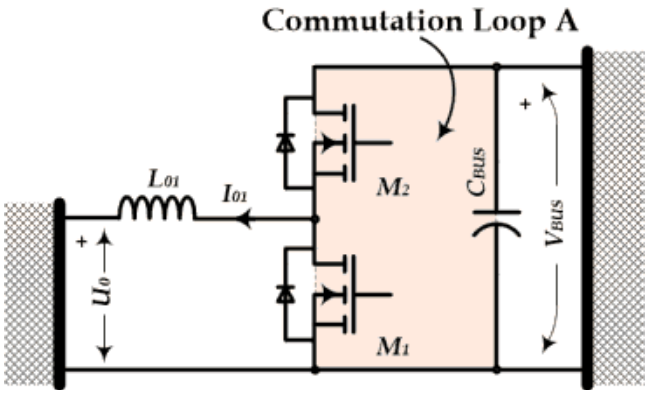
⇒ Better utilization of WBG Devices

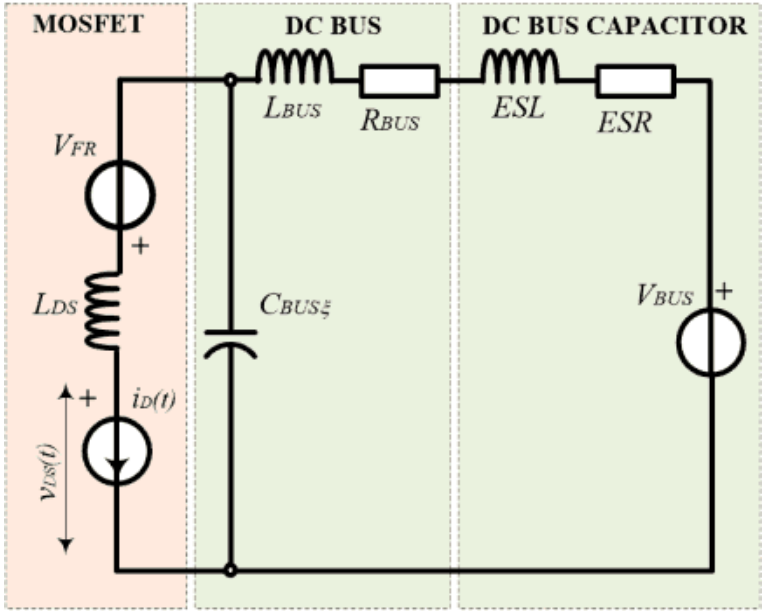
- Particularly case in low voltage high current applications
  - Even today with Si MOSFETs
  - In near future much more with WBG, particularly GaN

Multi-Cell Converters

-Synergy with new Power Semiconductors-

A Basic switching Cell





The Switch Voltage Rating

A. Steady state
   1. Dc bus voltage,

B. Transient Over-voltage
   2. Total Commutation inductance,
   3. Commutation di/dt,
   4. Number of Cells N
   5. Forward recover voltage,
   6. Effect of resonance

An Equivalent Model

$$V_{DS} = V_{BUS} + \underbrace{k_R \frac{L_\zeta}{N} \frac{di_D}{dt} + V_{FR}}_{TRANSIENT}$$

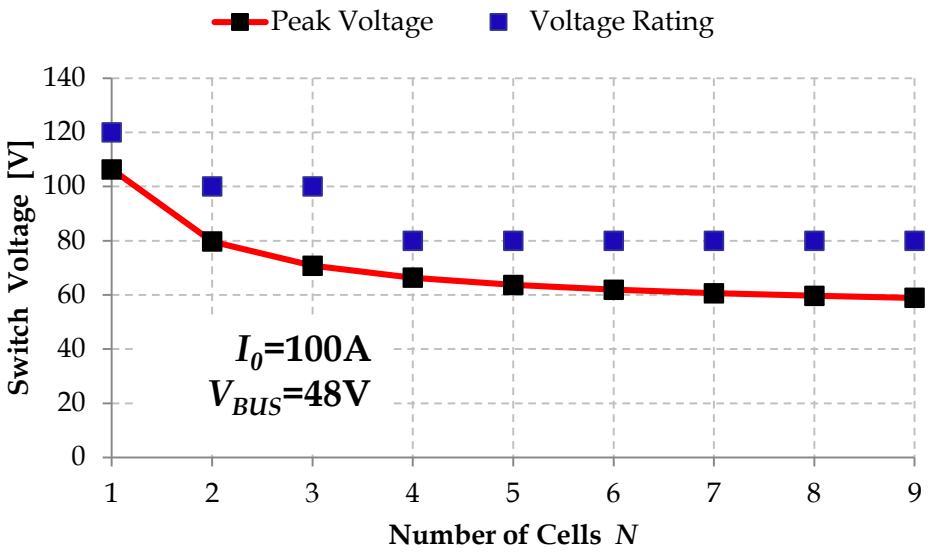
The Switch Total Voltage

Multi-cell Converters

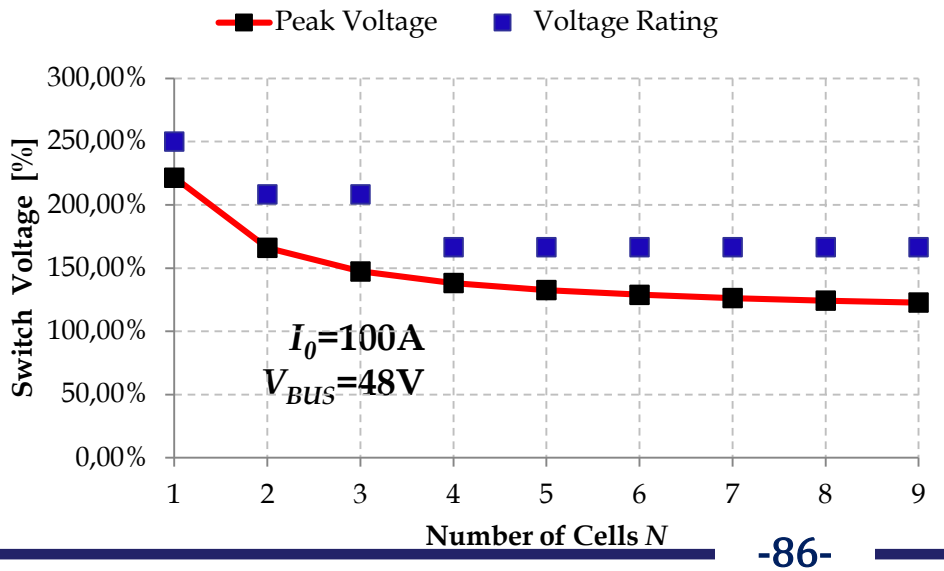
$$V_{DS} = V_{BUS} + \underbrace{k_R \frac{L_\zeta}{N} \frac{di_D}{dt}}_{TRANSIENT} + V_{FR}$$

Equivalent commutation inductance is reduced with number of cells N

- **Only way to go beyond the limit of Si**
- **and ...use full benefit of WBG...**



$$\frac{V_{DS}}{V_{BUS}} = 1 + \left[\underbrace{k_R \frac{L_\zeta}{N} \frac{di_D}{dt}}_{TRANSIENT} + V_{FR} \right] \frac{1}{V_{BUS}}$$

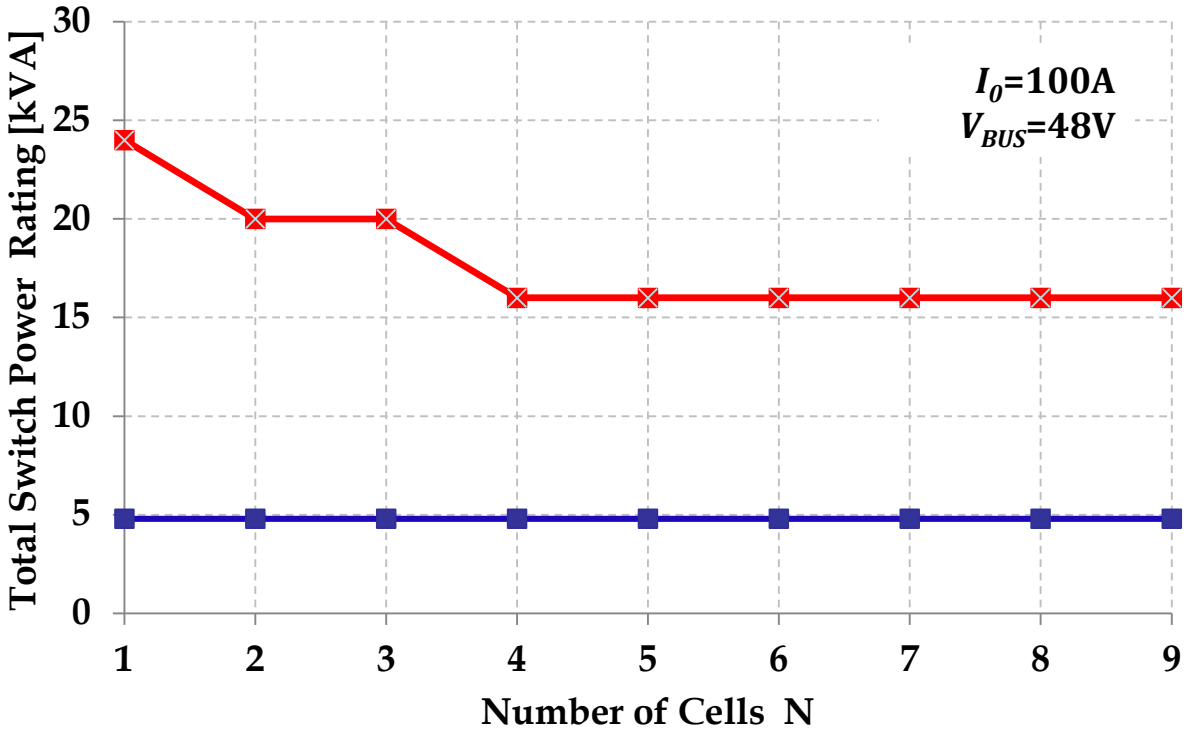


The Switch Relative (Normalized) Voltage

Multi-cell Converters

Total Power of all Semiconductors Switch

$$\sum_{1}^{N_{SW}} S_{(j)} = SN_{SW} = 2\left(V_{BUS} + k_R L_\zeta \frac{1}{N} \frac{di_D}{dt} + V_{FR} \right) I_0$$



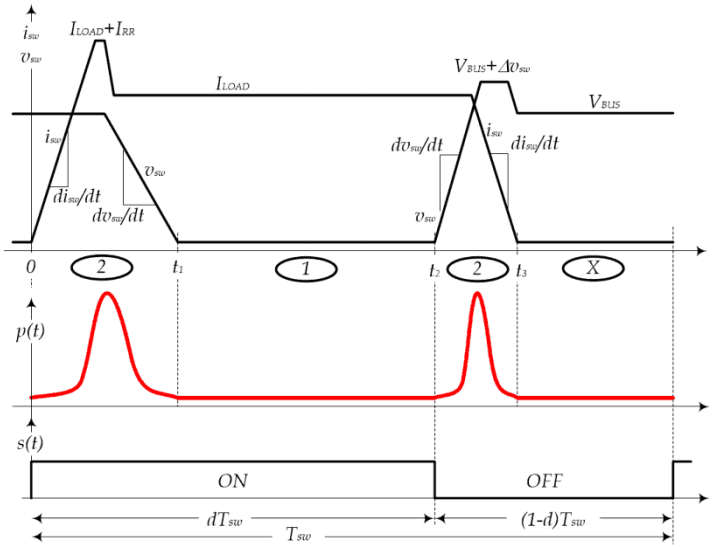
Multi-cell Converters

1. Conduction Losses

$$P_{CON} = \frac{I_0^2}{N} R_{DS(N)}$$

2. The Switch Commutation Losses

i. Voltage/Current overleaping
ii. Parasitic Inductance Energy
iii. Parasitic Capacitance Energy



$$P_{SW} \cong \left\{ \underbrace{V_{BUS} I_0 \frac{\left(t_{iF} + t_{vR} + t_{iR} + t_{vF}\right)}{2}}_{i} + \underbrace{\frac{1}{2} L_\zeta}_{ii} \frac{I_0^2}{N} + \underbrace{N \frac{1}{2} V_{BUS}^2 C_{OSS}}_{iii} \right\} f_{SW}$$

3. The FWD Commutation Losses

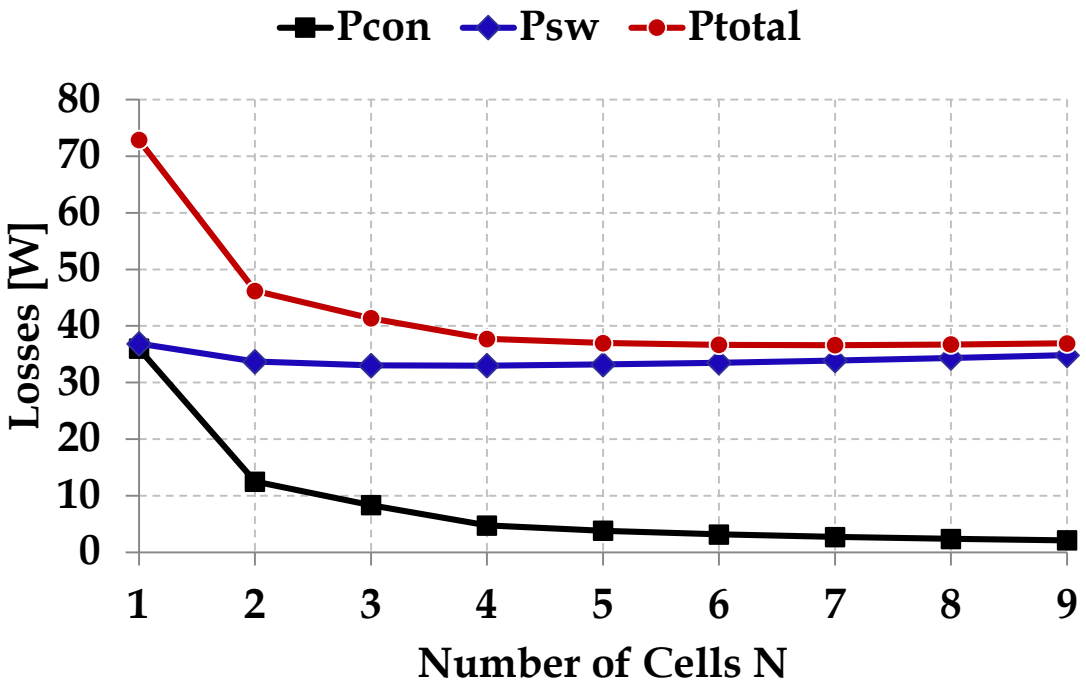
$$P_D \cong \left\{ V_{BUS} I_0 \frac{E_Q}{U_N I_N} \right\} f_{SW}$$

Multi-cell Converters

- f_{SW} =Constant
- Δi_0= Constant

Size (Cost) of the Filter ↓↓

$$L_0 = \frac{V_{BUS}}{f_{SW} N 4 \Delta i_{0\max}}$$



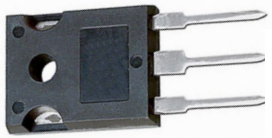
MOSFET losses versus number of levels *N*.

- **The dc bus voltage V_{BUS}=48V,**
- **The load current I_0=100A,**
- **The switching frequency is constant f_{SW}=100kHz.**

WBG Devices

Simplified linear model

$$\frac{di_D}{dt} = \frac{\frac{I_0}{g_m} + V_{GS(TH)} + |V_{EE}|}{\frac{R_G C_{ISS}}{g_m} + \frac{L_S}{N}} = k_0 + k_1 I_0 + k_2 |V_{EE}|$$



- $V_{GS(TH)}$=1-2V
- TO247 or TO220 Package
  - di/dt <0.5kA/µs ⇒ t_F>400ns @200A
- Even TO 252 and similar package makes no big difference

What is The Solution

I. Reduce the Inductance *Ls*
   - Lead-less package is MUST

II. Reduced current per a chip
   - Interleaving

III. Negative gate-source voltage V_{EE}

We need to explore existing topologies and use them in different way

a) Partial Power Processing Converters

b) Current Source Converters

c) Multi-Cell & **Multi-Level Converters**

d) Quantum Mode Resonant Converters

Multi-level Converters

-Split the input (capacitor) voltage into segments-

Multi-level Converters

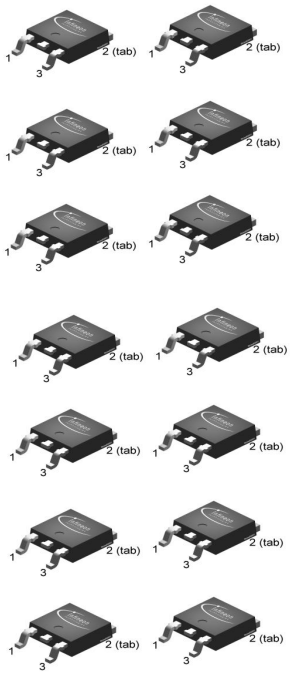
Why we need to split the input (dc bus) voltage into segments?

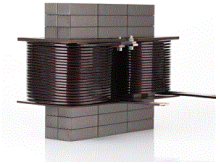
I. Good topic for (university) research,
II. Can we do something for passives (Inductors & Capacitors)?
III. Something else?
IV. And, is it a logical step?

Multi-level Converters

We need an Inductor-free converter…

- No additional inductors or just very small one..parasitic stray inductance…





Multi-level Converters

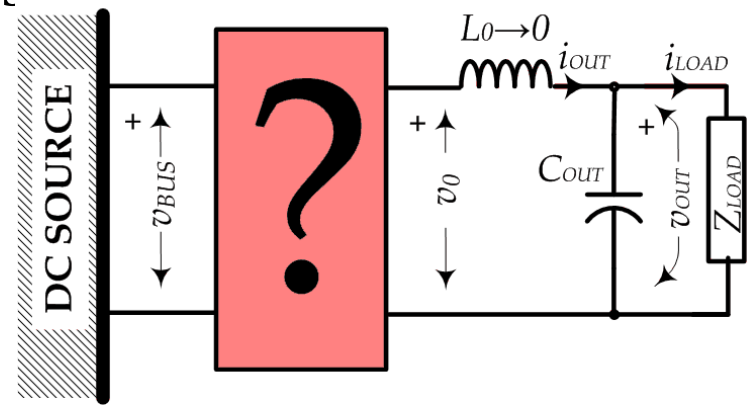
- An Inductor-free converter…no additional inductors or just very small one..parasitic stray inductance…
- The Inductance is proportional to flux
  - And the flux is volt-second on the inductor

$$L \approx \psi = \Delta v_{L0} \Delta T \approx \frac{\Delta v_0}{f_{SW}} k_{op}$$

A. Increase switching frequency f_{SW},
   - Nice, but not for free…switching los

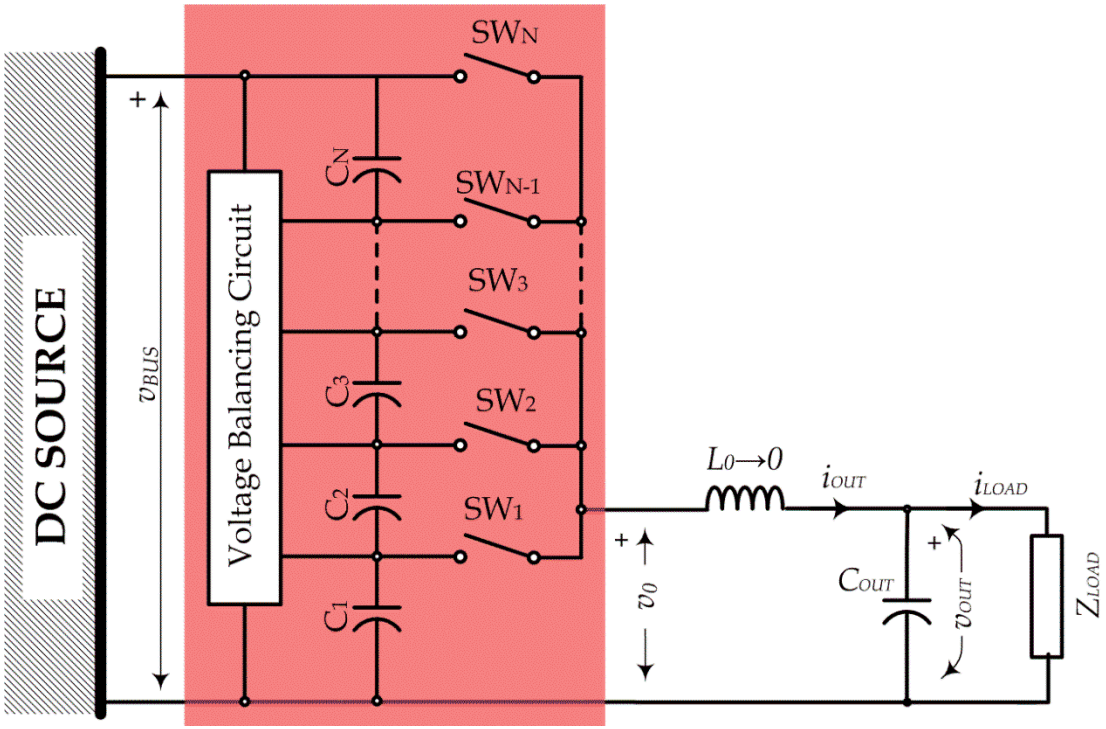
B. Reduce voltage step Δv_0,
   - Also nice, but how?

C. Or, can we play on k_{op}?
   - It looks possible, but how?



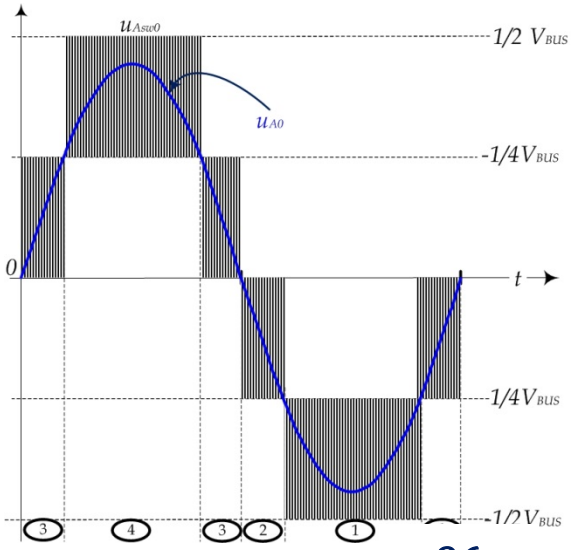
Multi-level Converters

- Instead of full dc bus voltage v_{BUS} on the filter
- We may apply the voltage in small steps
  - Multi-level power converters



$$L \approx \psi = \Delta v_{L0} \Delta T \approx \frac{\Delta v_0}{f_{SW}} k_{op}$$

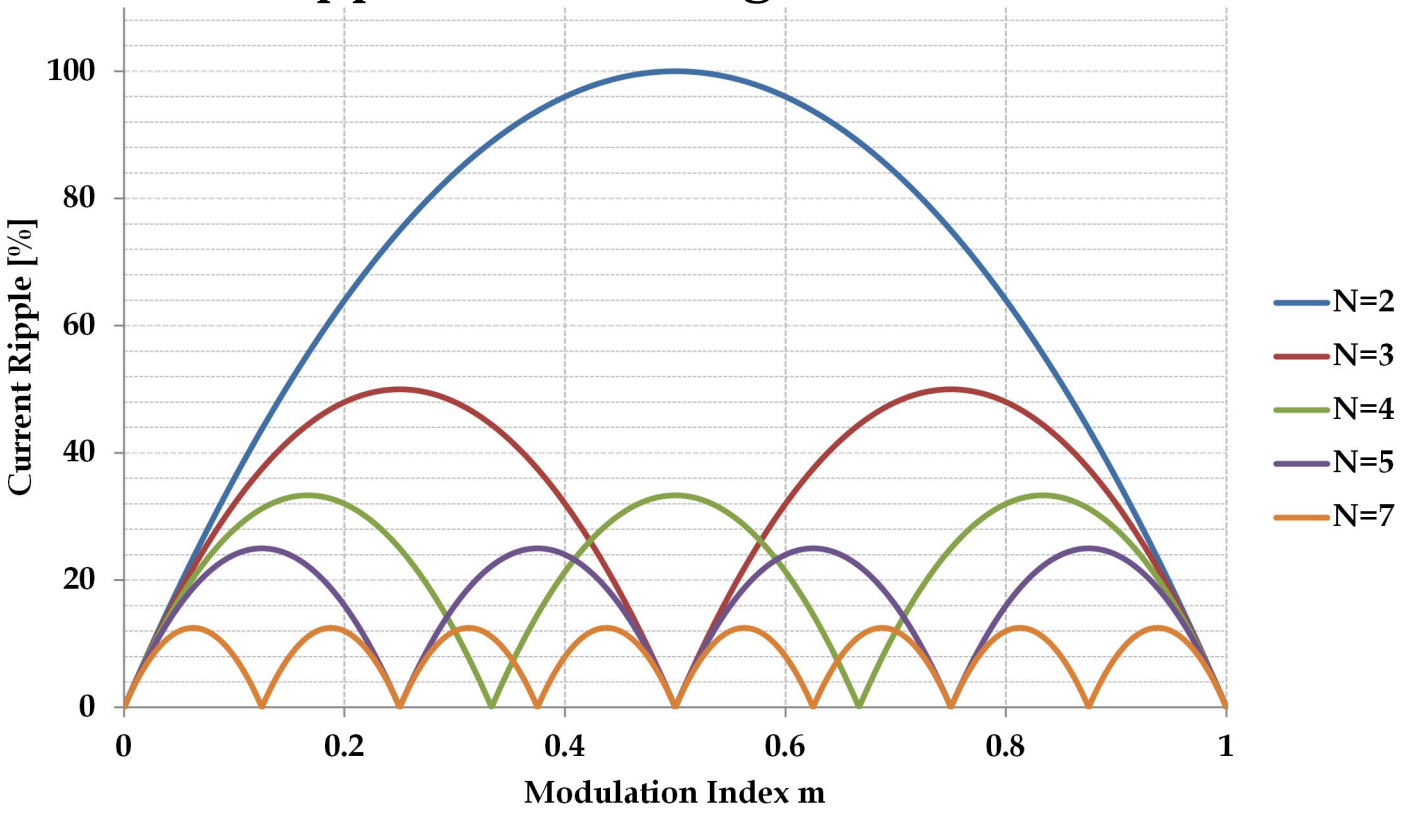
$$\Delta i_0 = \frac{V_{BUS}}{f_{SW} L_0 (N-1)} \left(d^2 - d\right)$$



Multi-level Converters

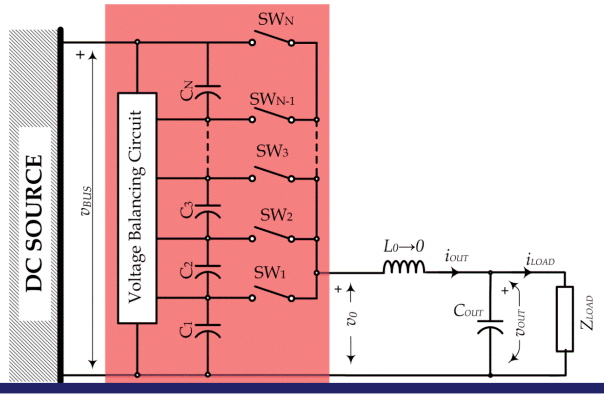
$$\Delta i_0 = \frac{V_{BUS}}{f_{SW} L_0 (N-1)} \left[((N-1)m - floor((N-1)m)) - ((N-1)m - floor((N-1)m))^2 \right]$$

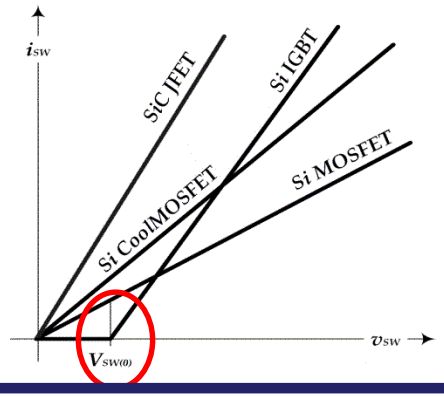
Current ripple overall range of modulation index m

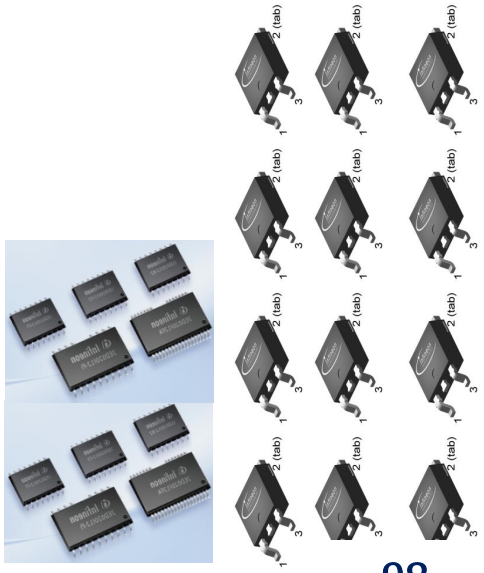


Multi-level Converters

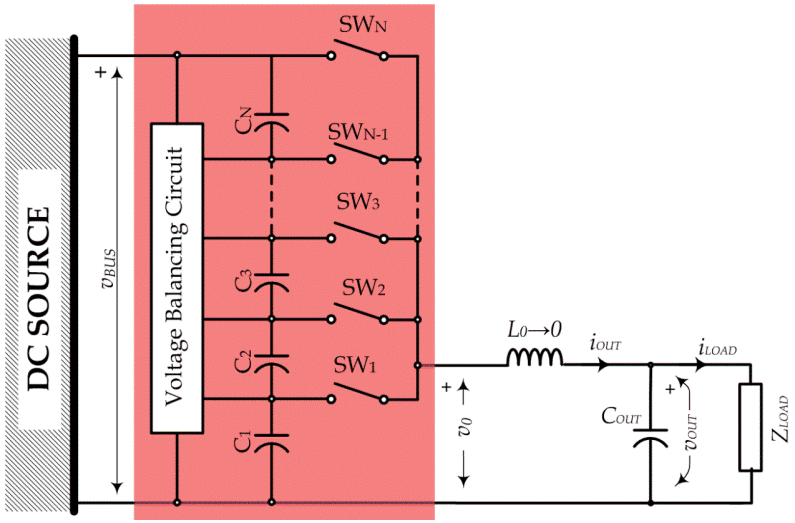
- Multi-level power converters are state of the art in high voltage high power applications
  - Not yet case in low voltage low power application
- What device ? Bipolar (IGBT) or Unipolar (MOSFET)?
- Low voltage Unipolar devices are preferred
  - CoolMOS, OptiMOS
- But, what topology?
- How to control such a complex converter?

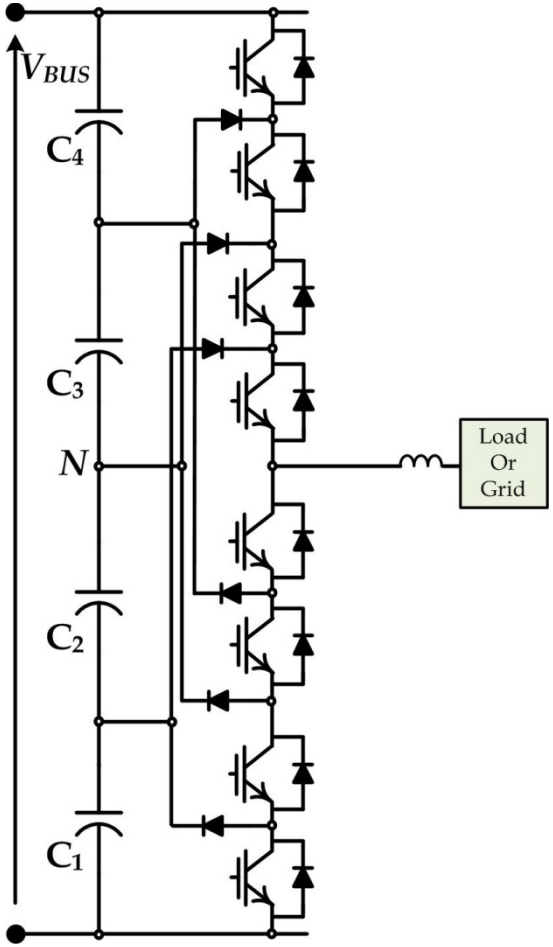




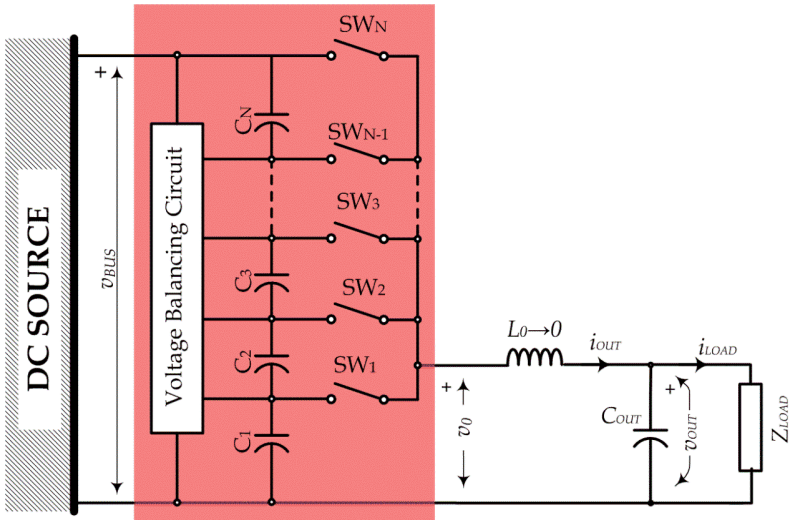


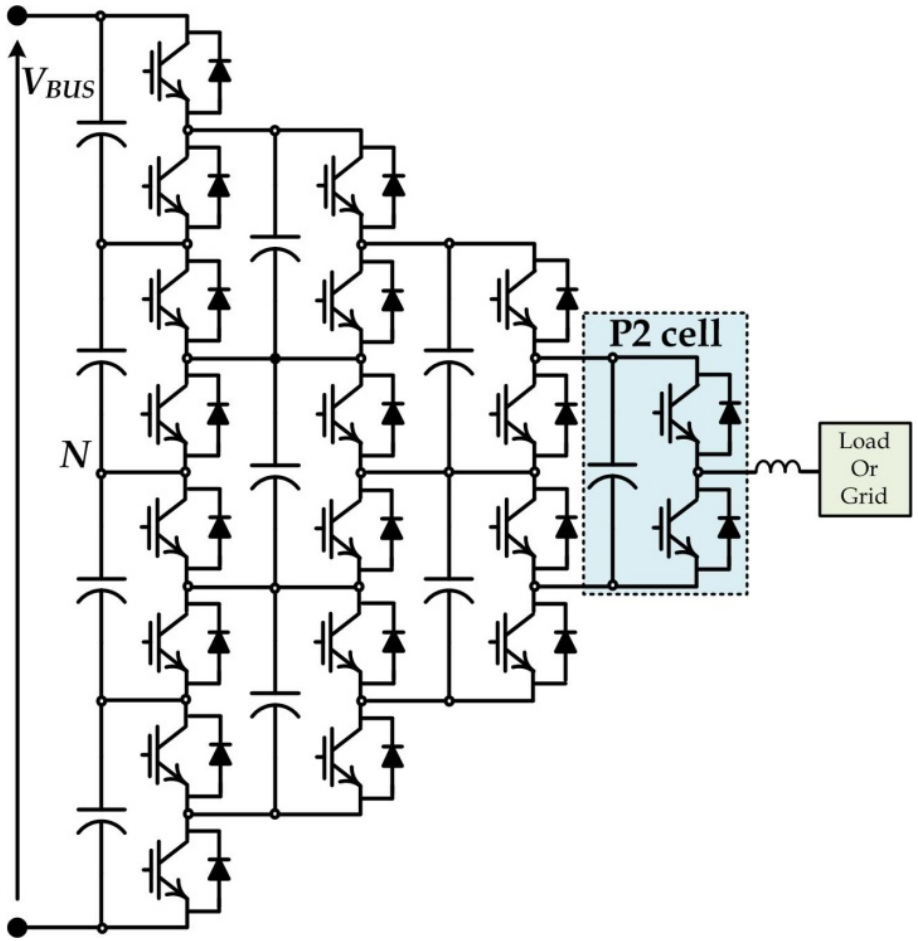
Multi-level Converters



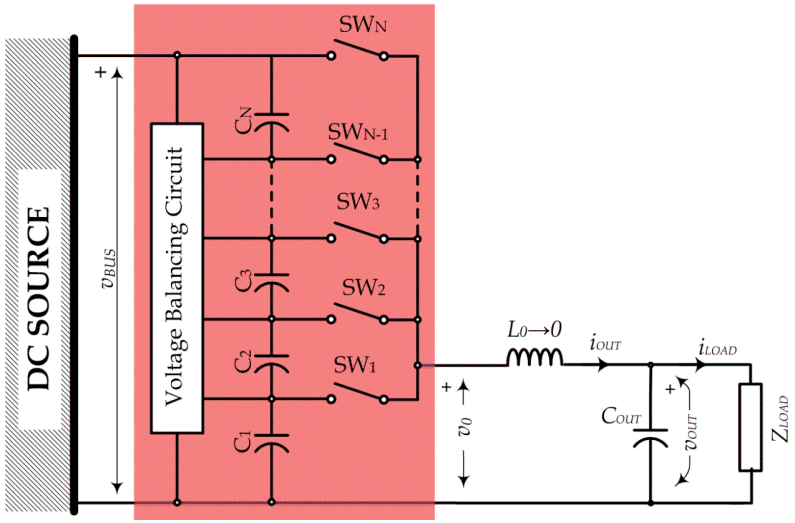


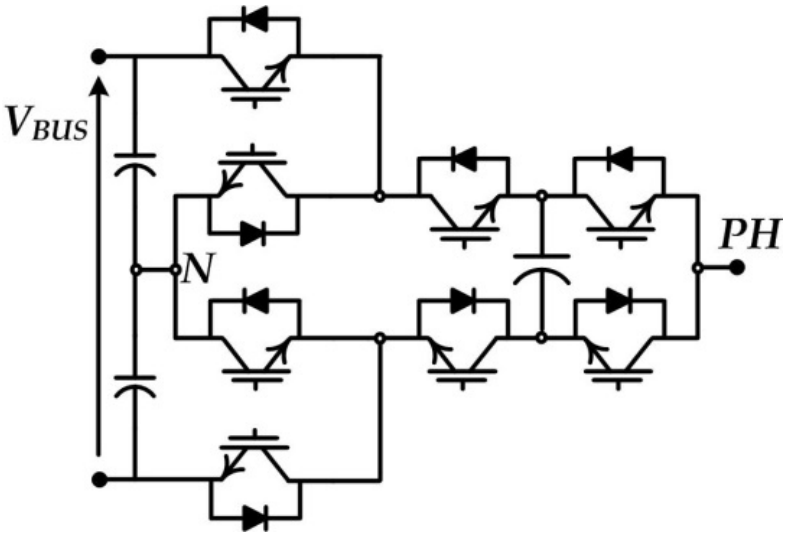
Multi-level Converters



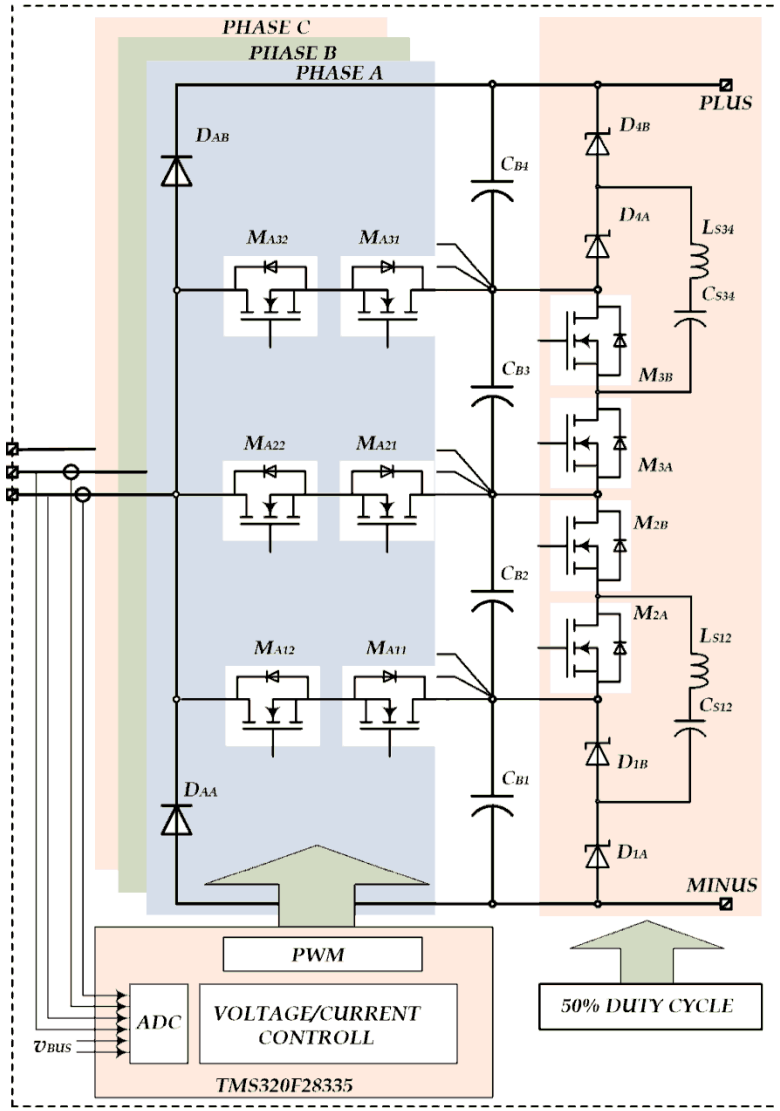


Multi-level Converters

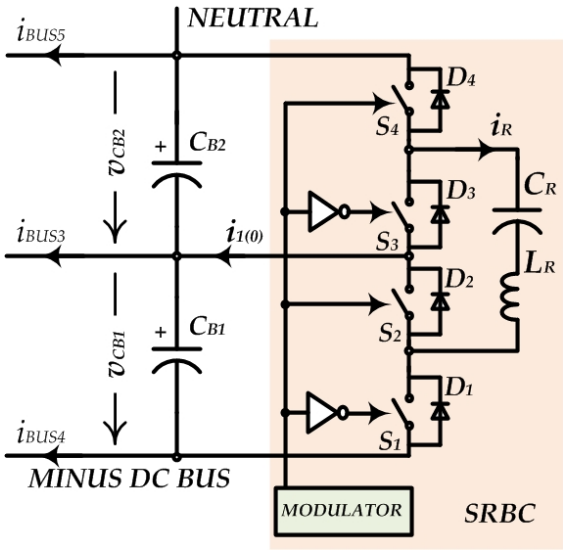




Multi-level Converters

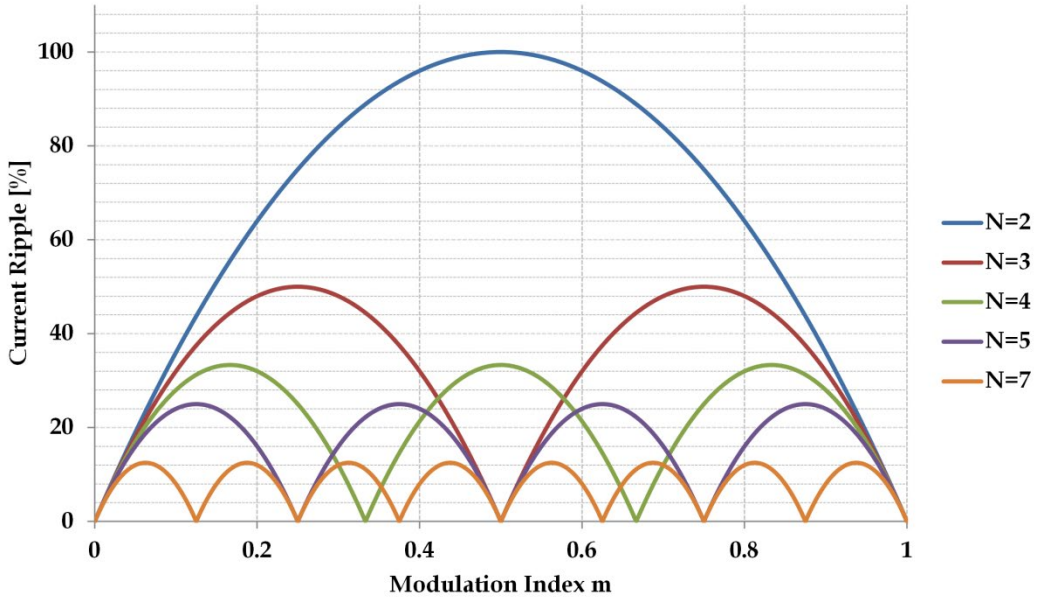


P. J. Grbović, F. Crescimbini, A. Lidozzi and L. Solero, "5-Level Unidirectional T-Rectifier for High Speed Gen-Set Applications," ECCE America 2014, Pittsburg, USA, 14-18 September, 2014.



Multi-level Converters

Multi-level ➡ Filter cost/size reduction



What ELSE?

Multi-level Converters

- **What about the load voltage and the load stress?**

C_P-The load parasitic capacitance

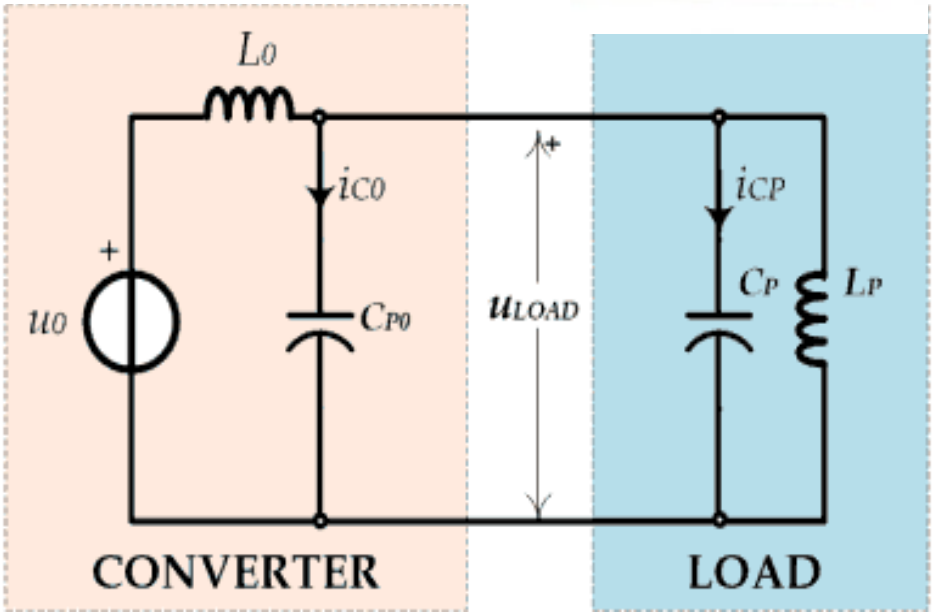
$$i_{CP} = C_P \frac{du_{LOAD}}{dt}$$

- **Just an indication,**
- **Much more complex in the reality,**

I. *dE/dt ≈ dv/dt* is critical for the load insulation
- *dv/dt should be <10kV/µs*

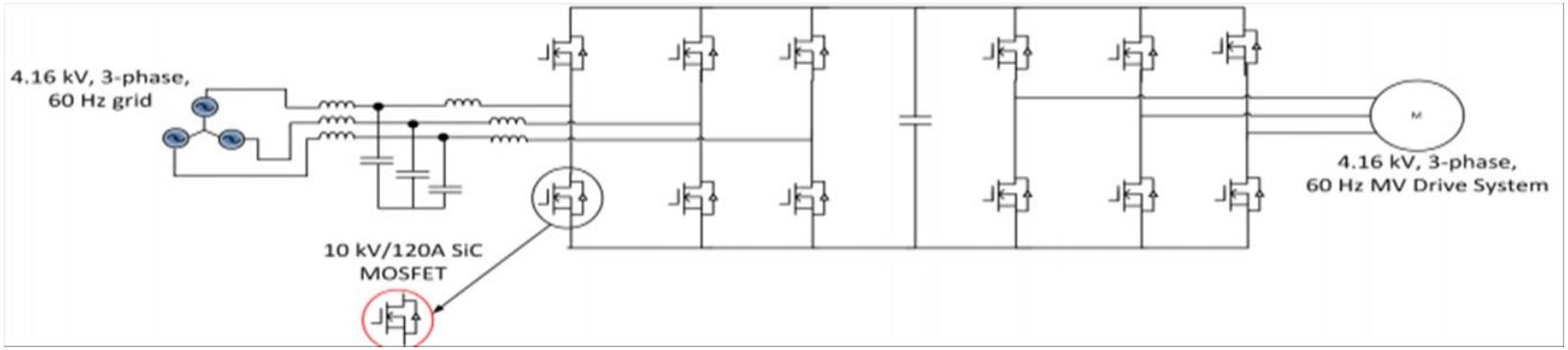
II. Voltage reflection

III. The machine shaft parasitic current



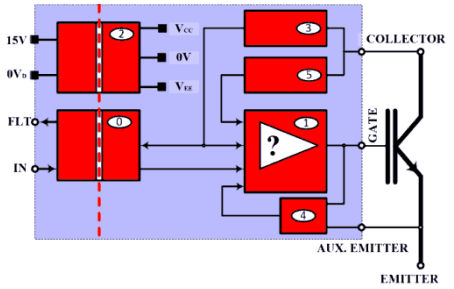
Multi-level Converters

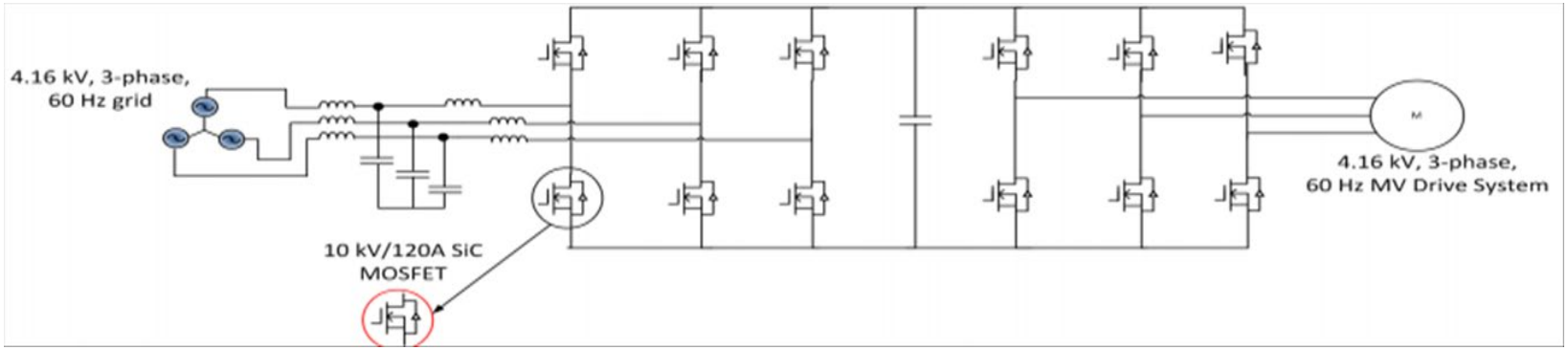
- **In general, electrical machines do not like high *dv/dt* stress**
- **BUT, what we are doing is completely opposite!!**
- A new WBG (SiC MOSFET) switch **10kV&120A @ 100-200ns**
  - ***30-100kV/µs***



Multi-level Converters

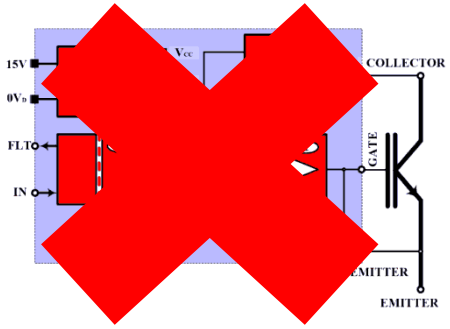
- Can we use an active gate driver and slowdown the switching?

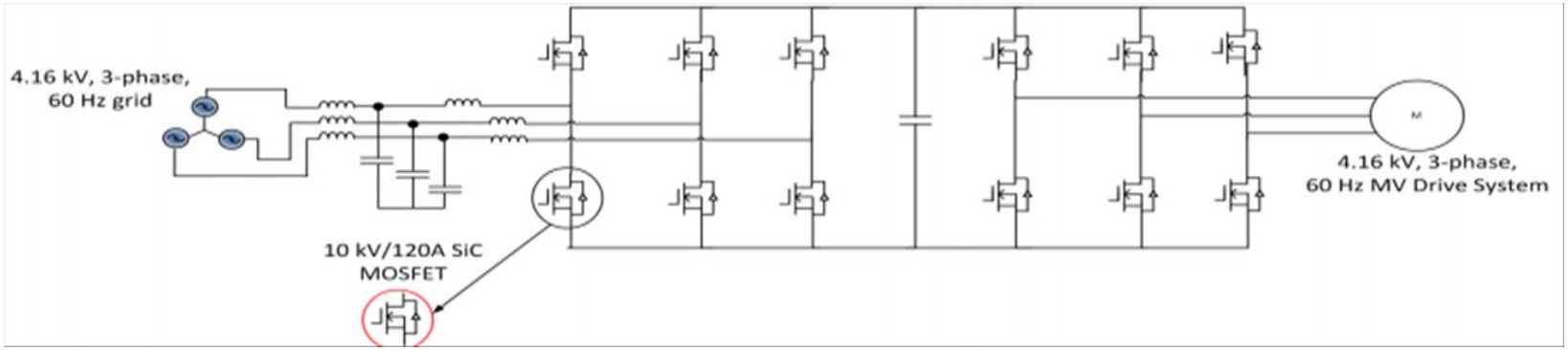




Multi-level Converters

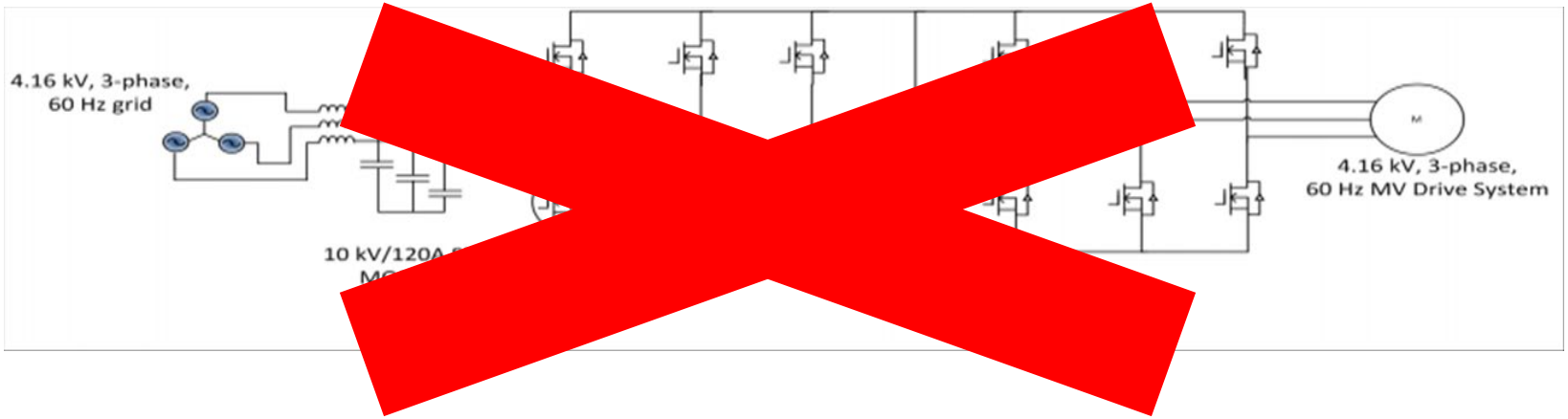
- Can we use an active gate driver and slowdown the switching?
- Yes, but it does not make sense!!





Multi-level Converters

- Can we use an active gate driver and slowdown the switching?
- Yes, but it does not make sense!!
- We Must split the dc bus voltage into segments and apply segment by segment on the load
  - Multi-level switching not 2-level switching



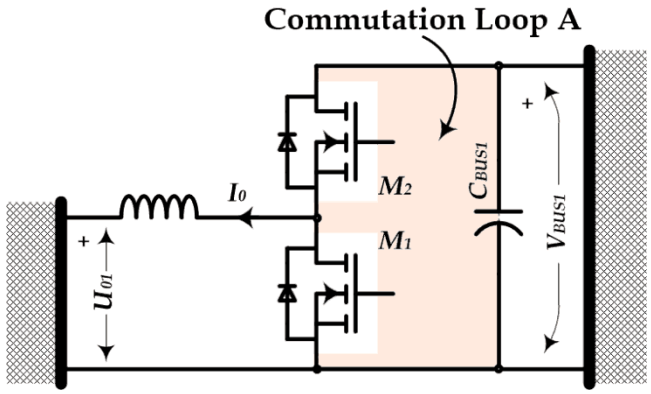
What about low-voltage high-current conversion?

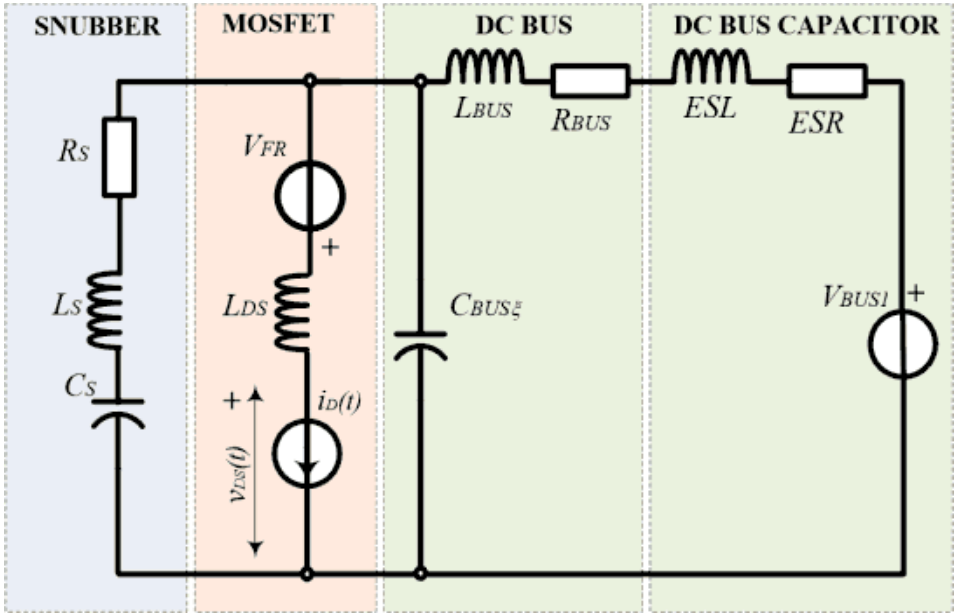
1) **Switch(s) Voltage Rating**
   - ❑ Select proper devices with proper voltage rating

2) **Switch(s) (Total) Power Rating**
   - ❑ What is total power of Semiconductors?
   - ❑ Is it optimal or not?
   - ❑ *N=x* or *N=y*, which one is better

3) **Conversion Losses**
   - ❑ Optimization: efficiency, size and cost?
   - ❑ *N=x* or *N=y*, which one is better

A Basic switching Cell





Small Signal Model

The Switch Voltage Rating

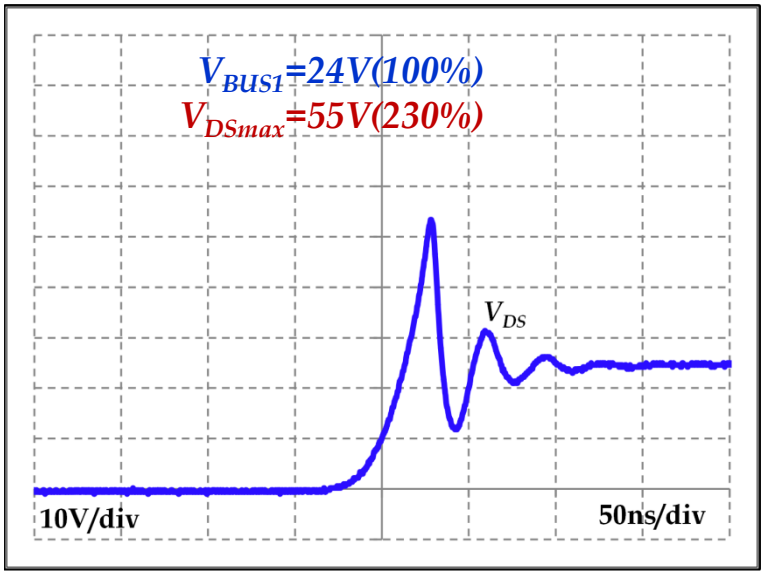
A. Steady state
   1. Dc bus voltage,
   2. Number of Levels

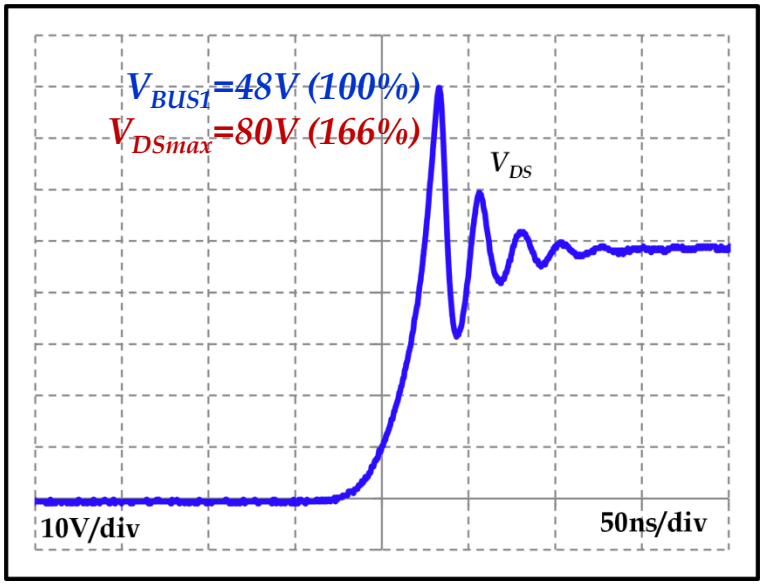
B. Transient Over-voltage
   3. Total Commutation inductance,
   4. Commutation di/dt,
   5. Forward recover voltage,
   6. Effect of resonance

$$V_{DS} = \frac{V_{BUS}}{(N-1)} + \underbrace{k_R L_\zeta \frac{di_D}{dt} + V_{FR}}_{TRANSIENT}$$

The Switch Total Voltage

Multi-level Converters





Experimental waveforms of drain source turn-off voltage v_{DS}

- **The cell dc bus voltage V_{BUS1}=24V (left) and V_{BUS1}=48V (right).**
- **OptiMOS PB019N08**
- **Load current I_0=150A**
- **Gate resistance R_G=1Ω,**
- **Gate driver off state voltage V_{EE}=-5V**

Multi-level Converters

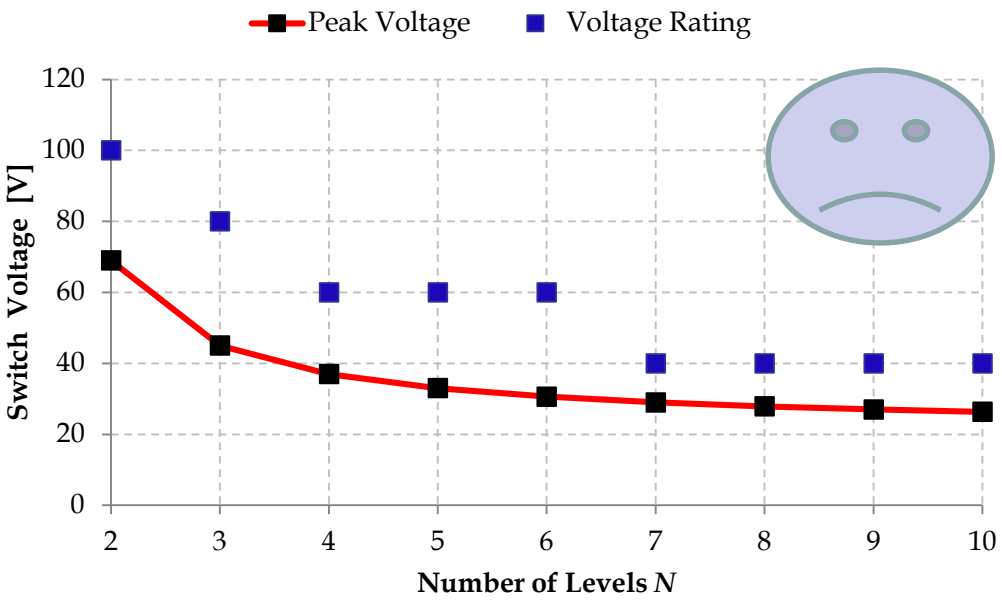
	V_{DS} [V]	R_{DS} [mΩ]	G_m [S]	t_F [ns]	t_R [ns]	C_{ISS} [nF]	C_{OSS} nF]
Maximum Drain Current I_D=180A		Source Inductance L_S=5nH			Forward Recovery Voltage V_{FR}=5V		
IPB009N03	30	0.95	370	26	22	20	6
IPB011N04	40	1.1	370	25	21	22	4.1
IPB016N06	60	1.6	245	35	38	21	3.3
IPB019N08	80	1.9	206	28	33	11	2.9
IPB025N10	100	2.5	200	34	28	11	2
IPB036N12	120	3.6	195	25	21	10.5	1.3

Switch peak voltage and the switch rating versus number of levels *N*.

- V_{BUS}=48V
- I_0=100A

N>6, the voltage rating constant!

- **Defined by the over-voltage not the number of levels N**



Multi-level Converters

	V_{DS} [V]	R_{DS} [mΩ]	G_m [S]	t_F [ns]	t_R [ns]	C_{ISS} [nF]	C_{OSS} nF]
Maximum Drain Current I_D=180A		Source Inductance L_S=5nH			Forward Recovery Voltage V_{FR}=5V		
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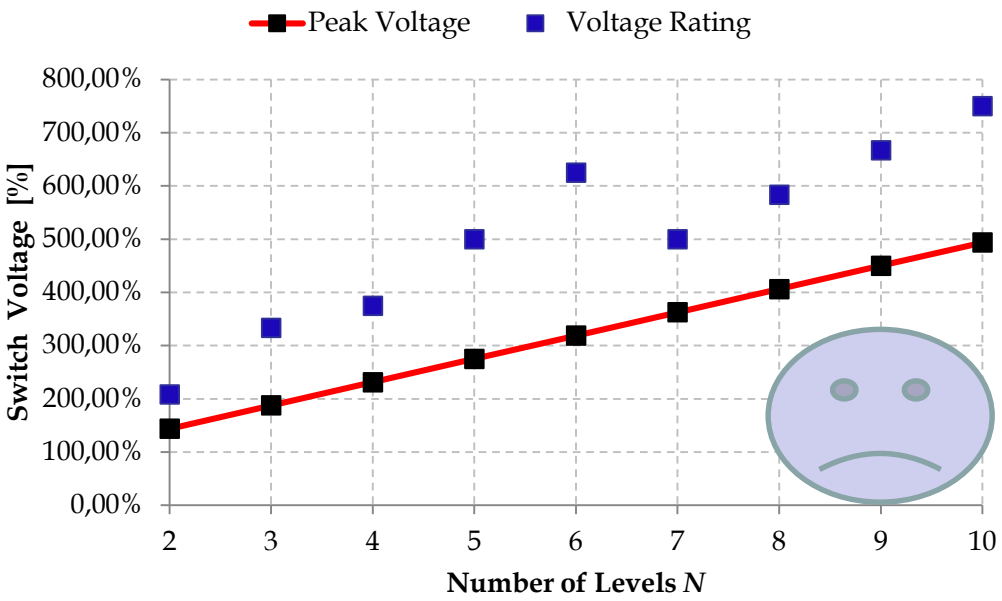
IPB025N10	100	2.5	200	34	28	11	2
IPB036N12	120	3.6	195	25	21	10.5	1.3

The Switch normalized peak voltage =f(*N*).

$$\frac{V_{DS}}{\frac{V_{BUS}}{(N-1)}} = 1 + \left[\underbrace{k_R L_\zeta \frac{di_D}{dt} + V_{FR}}_{TRANSIENT} \right] \frac{(N-1)}{V_{BUS}}$$

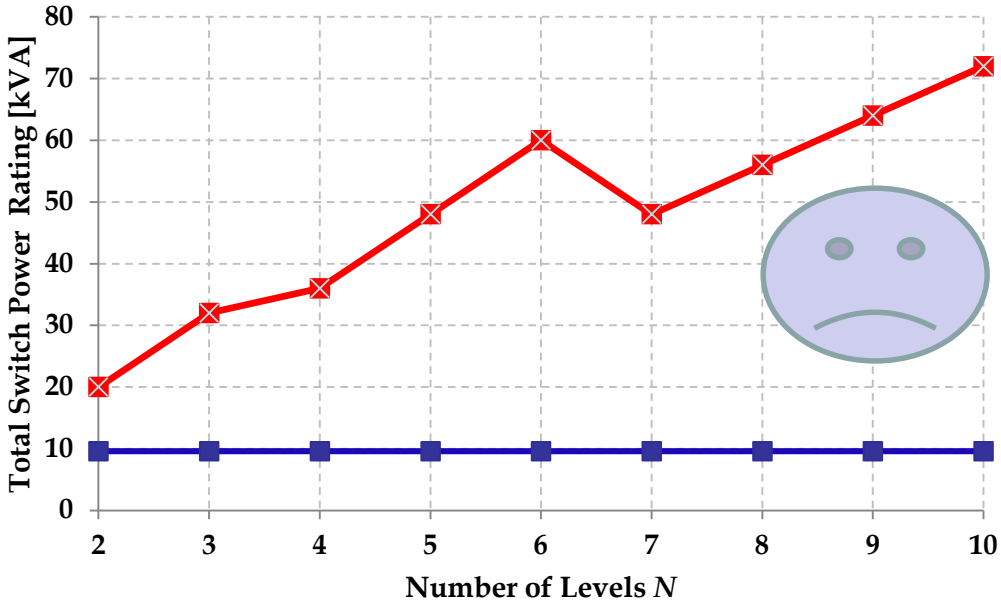
- V_{BUS}=48V
- I_0=100A



Multi-level Converters

Total Power of all Semiconductors Switch

$$\sum_{1}^{N_{SW}} S_{(j)} = SN_{SW} = 2(N-1)\left(\frac{V_{BUS}}{(N-1)} + k_R L_\zeta \frac{di_D}{dt} + V_{FR}\right) I_0$$



- I_0=100A
- V_{BUS}=48V

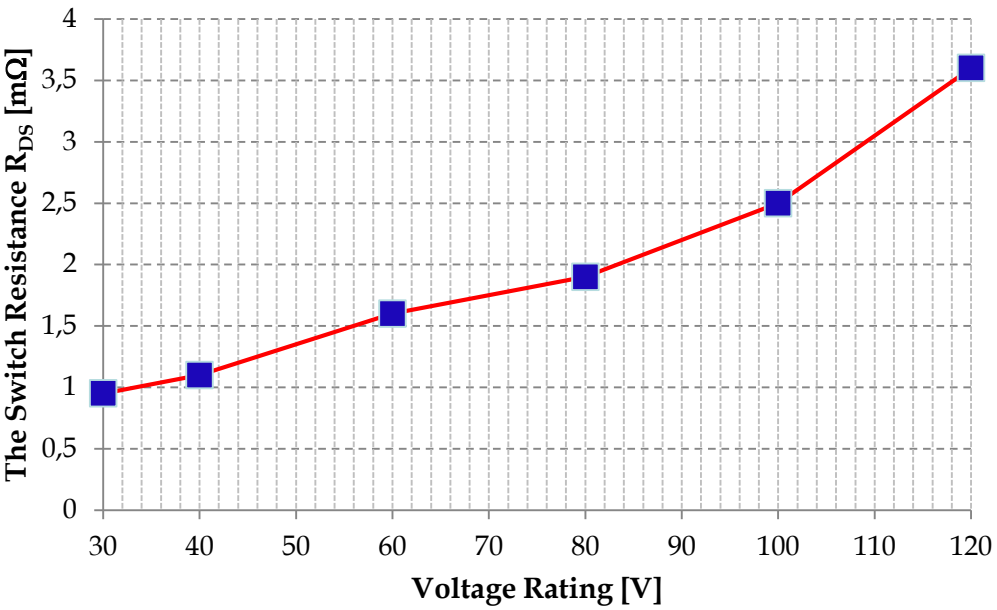
Is this correct?
Not completely, but it gives an indication….

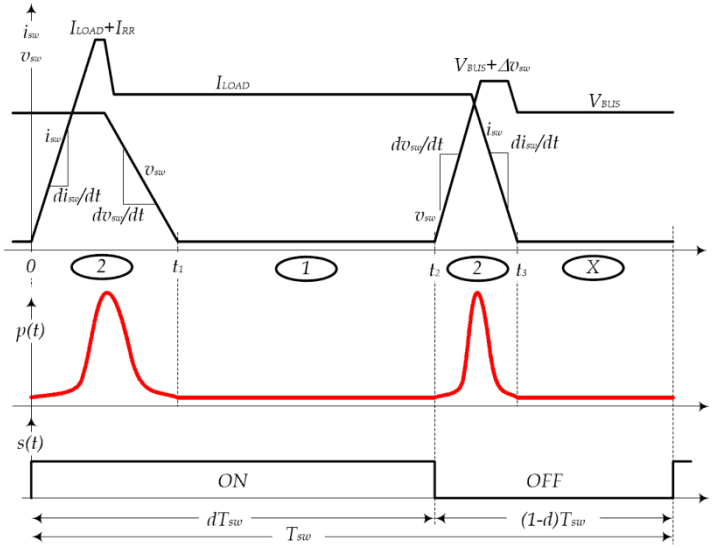
Multi-level Converters

1. Conduction Losses

$$P_{CON} = (N-1) I_0^2 R_{DS(N)}$$

- Depend on number of Levels *N*
  - R_{DS}= *Function* (The blocking voltage)





Low voltage MOSFET resistance R_{DS} versus rated voltage.

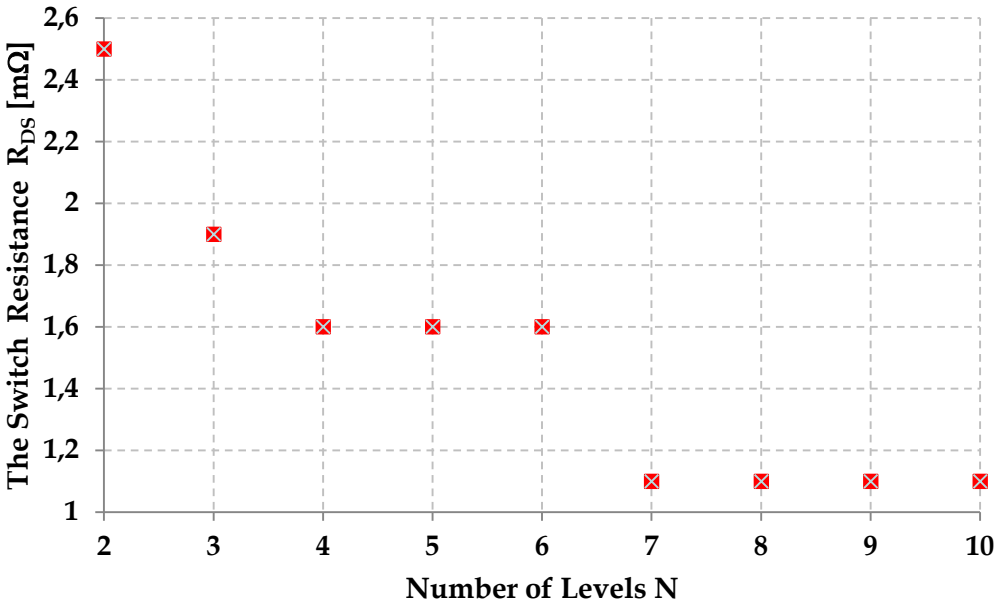
- **Infineon OptiMOS family**

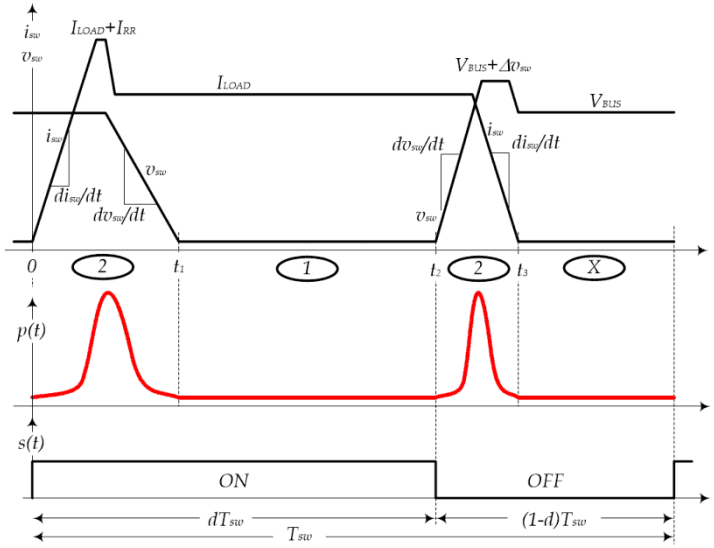
Multi-level Converters

1. Conduction Losses

$$P_{CON} = (N-1) I_0^2 R_{DS(N)}$$

- Depend on number of Levels *N*
  - R_{DS}= *Function* (The blocking voltage)
  - The blocking voltage=*Function* (*N*)





Low voltage MOSFET resistance R_{DS} versus number of levels N.

- Infineon OptiMOS family,
- V_{BUS}=48V

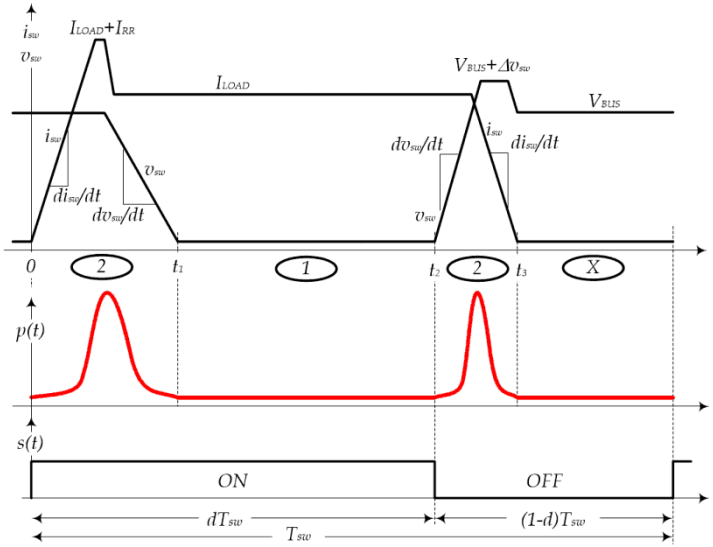
Multi-level Converters

1. Conduction Losses

$$P_{CON} = (N-1) I_0^2 R_{DS(N)}$$

2. The Switch Commutation Losses

i. Voltage/Current overleaping
ii. Parasitic Inductance
iii. Parasitic Capacitance



$$P_{SW} \cong \left\{ \underbrace{\frac{V_{BUS}}{(N-1)} I_0 \frac{(t_{iF}+t_{vR}+t_{iR}+t_{vF})}{2}}_{i} + \underbrace{\frac{1}{2} L_\zeta I_0^2}_{ii} + \underbrace{\frac{1}{2}\left[\frac{V_{BUS}}{(N-1)}\right]^2 C_{OSS}}_{iii} \right\} f_{SW}$$

3. The FWD Commutation Losses

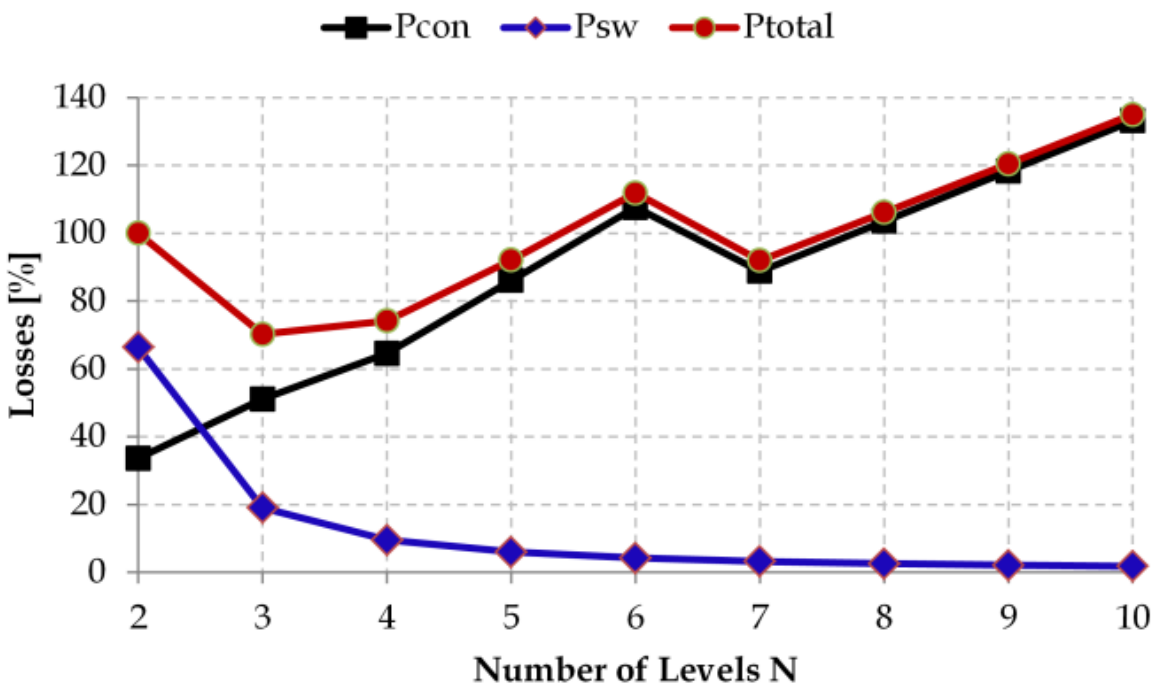
$$P_D \cong \left\{ \frac{V_{BUS}}{(N-1)} I_0 \frac{E_Q}{U_N I_N} \right\} f_{SW}$$

Multi-level Converters

Machine (HS-PMSG)

- L_0=Constant
- f_{SW} can be scaled (reduced) to constant current ripple Δi_0

$$f_{SW} = \frac{V_{BUS}}{L_0 (N-1) 4 \Delta i_{0\max}}$$



MOSFET losses versus number of levels *N*.

- V_{BUS}=48V,
- I_0=150A,
- The switching frequency is scaled to constant current ripple Δi_0=20A.

We need to explore existing topologies and use them in different way

a) Partial Power Processing Converters

b) Current Source Converters

c) **Multi-Cell & Multi-Level Converters**

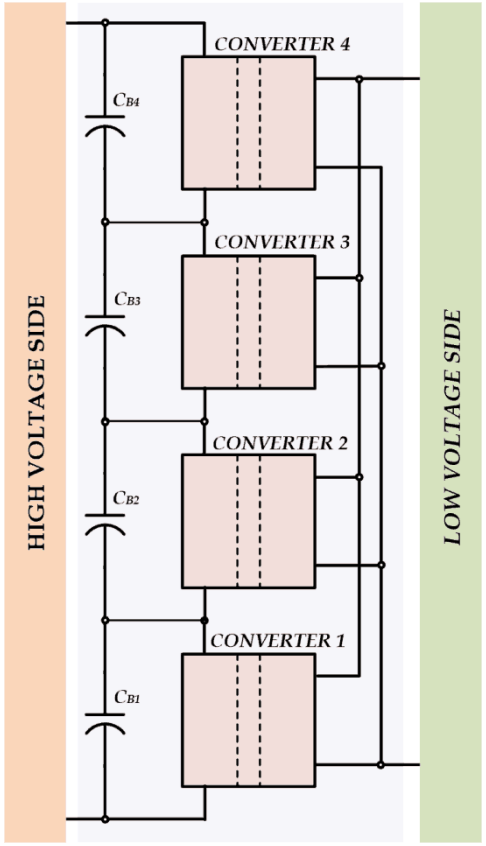
d) Quantum Mode Resonant Converters

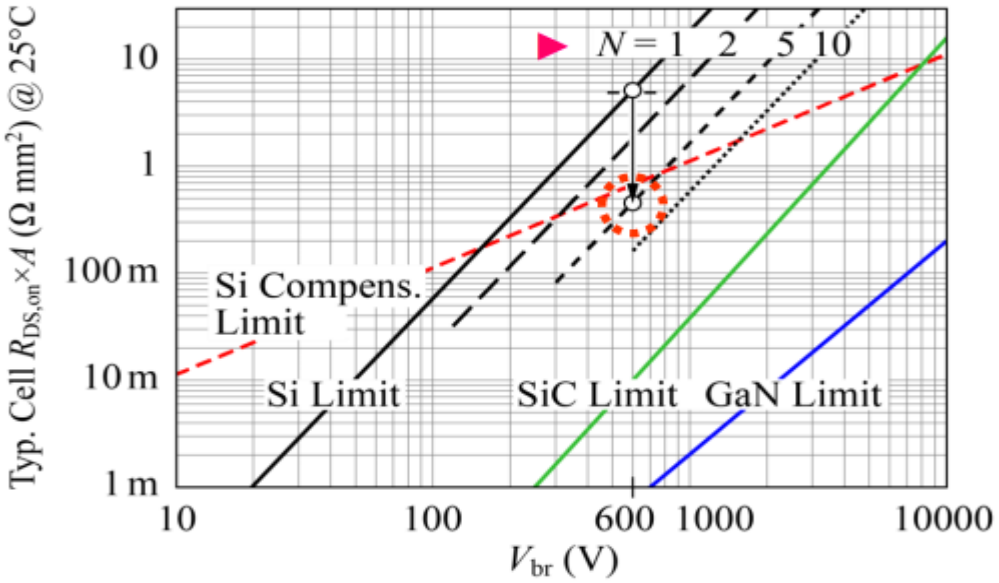
Multi-Cell & Multi-Level

-ISOP, IPOS,….-

Multi-level/cell Converters

- **High Voltage Side-Series connected converters**
- **Low Voltage Side-Parallel connected converters**

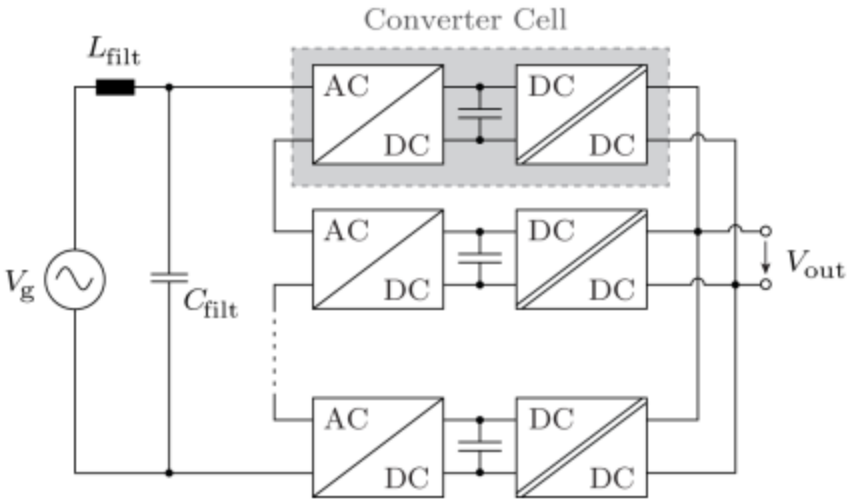


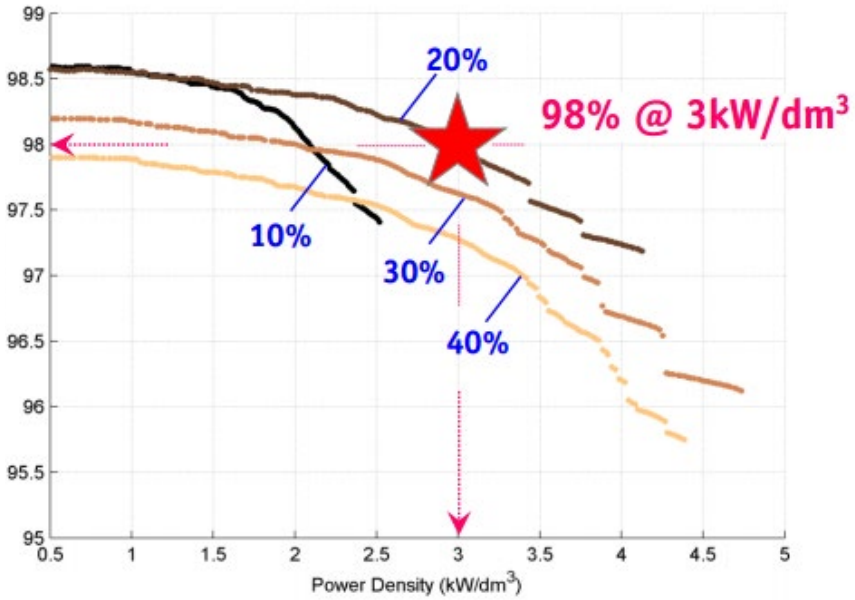


This is only way to go beyond limit of Si devices…

Multi-level/cell Converters

- ISOP based Ultra efficient and compact Telecom power supply

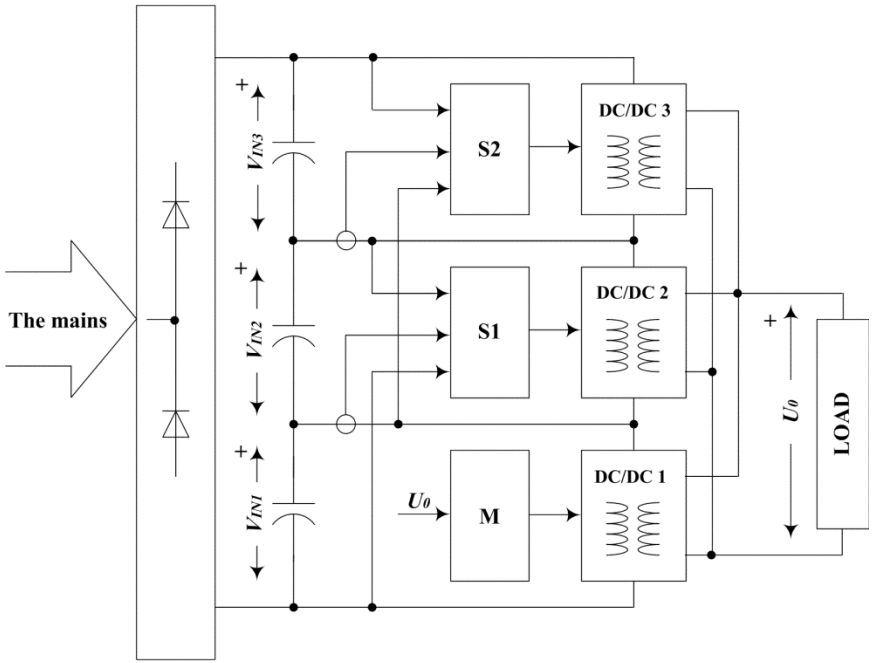




M. Kasper, J. W. Kolar and G. Deboy, "98.5% / 1.5kW/dm³ Multi-Cell Telecom Rectifier Module (230VAC/48VDC) –Breaking the Pareto Limit of Conventional Converter Approaches" ECPE Workshop "Advanced Multi-cell / Multi-level Power Converters", 1-2 July, 2014, Toulouse, France

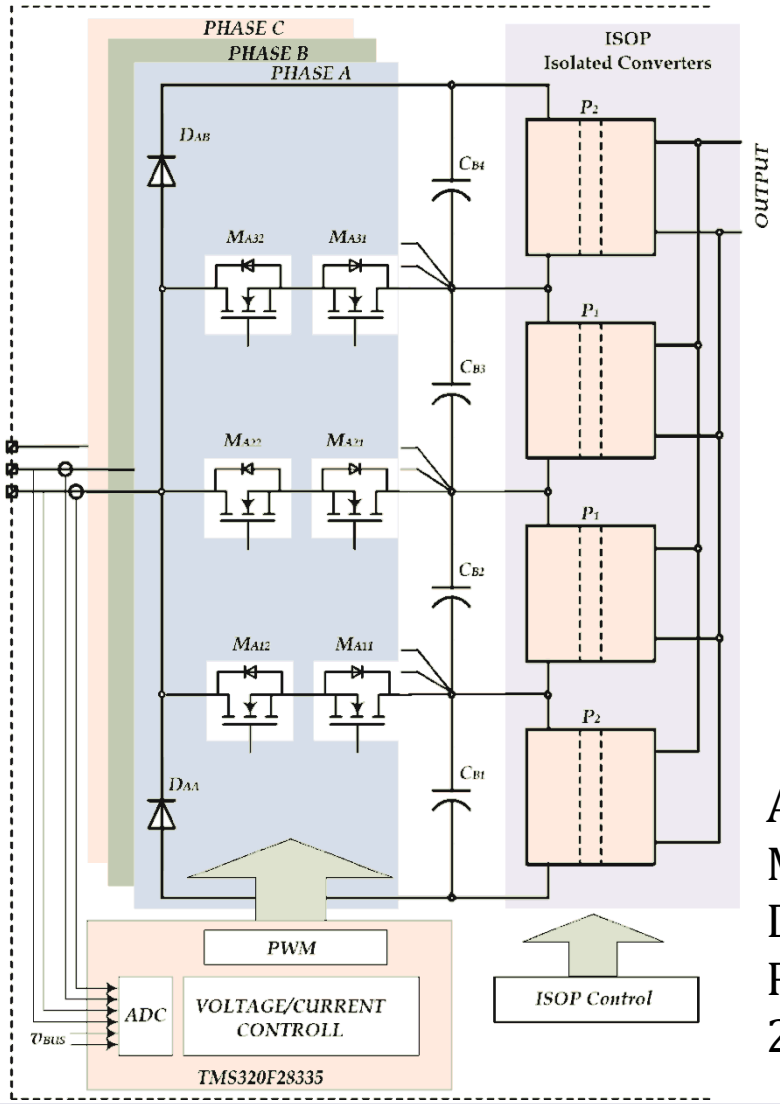
Multi-level/cell Converters

Low Cost Auxiliary power supply based on ISOP Concept



P. J. Grbović, "Input Serial Output Parallel (ISOP) Connected High Voltage Power Supplies Based on Simple Master/Slave Control Technique", *IEEE Trans. Power Electronics*, Vol. 24, No. 2, pp. 316-328, February 2009

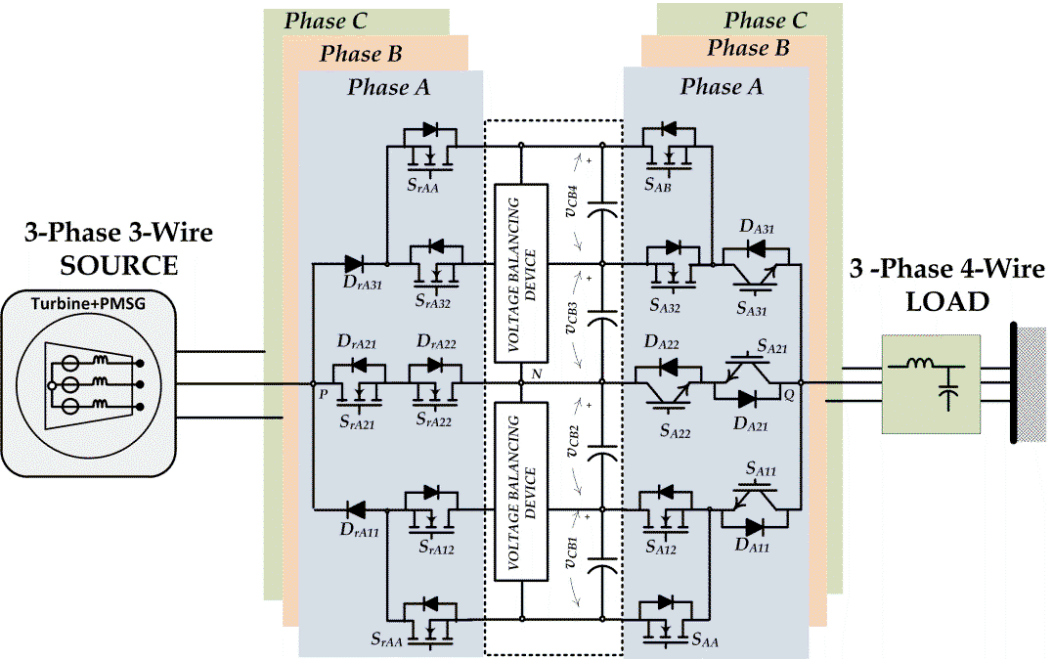
Multi-level/cell Converters

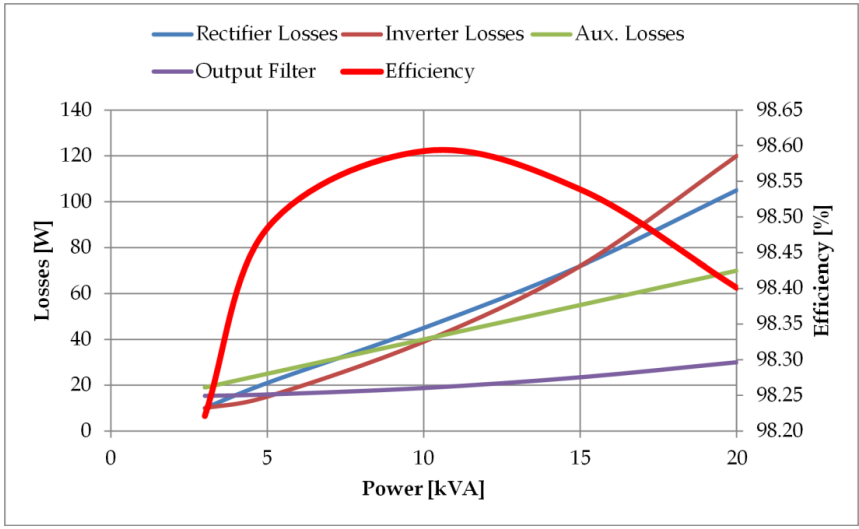


ISOP DC-DC Converter for Aerospace Applications

Alessandro Lidozzi, **Petar J. Grbović**, Luca Solero, Marco Di Benedetto and Stefano Bifaretti, "ISOP DC-DC Converters Equipped 5-Level Unidirectional T-Rectifier for Aerospace Applications" ECCE America 2015, Montreal, Canada, 20-24 September, 2015.

Multi-level/cell Converters





- P. J. Grbović , M. Di Benedetto, L. Solero, F. Crescimbini and A. Lidozzi, " **5-Level E-Type Back to Back Power Converters:** ***A New Solution for Extreme Efficiency and Power Density*** "
  - **98.5% Double Conversion Efficiency**
  - **5.3kW/dm³**
  - **5kVA/kg**
  - **Si Devices Only (no WBG)**

At the End, Multi-Level…Multi-Cell…ISOP…

Is it easy and good as it looks like??

Some Issues

Multi-Cell & Multi-level Conversion will solve all our issues….**or may be not**….

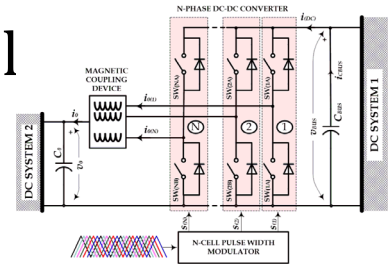
- 120V OptiMOS for 3 phase 400V system
  - **Very low losses**
  - **Very popular and low cost device**

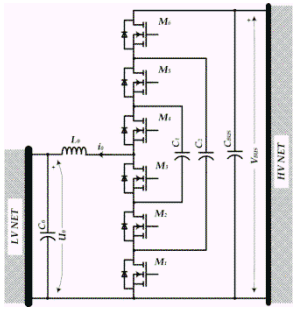
How many devices we need per a system?

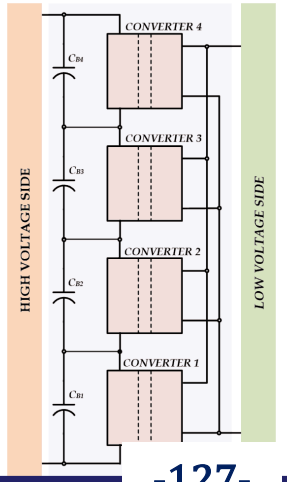
I. **2x10=20 per phase and cell**

II. **2 cells & 3 phases converter** → **120 devices per a converter**

III. **Back to back Config. system** → **240 Devices per a system**



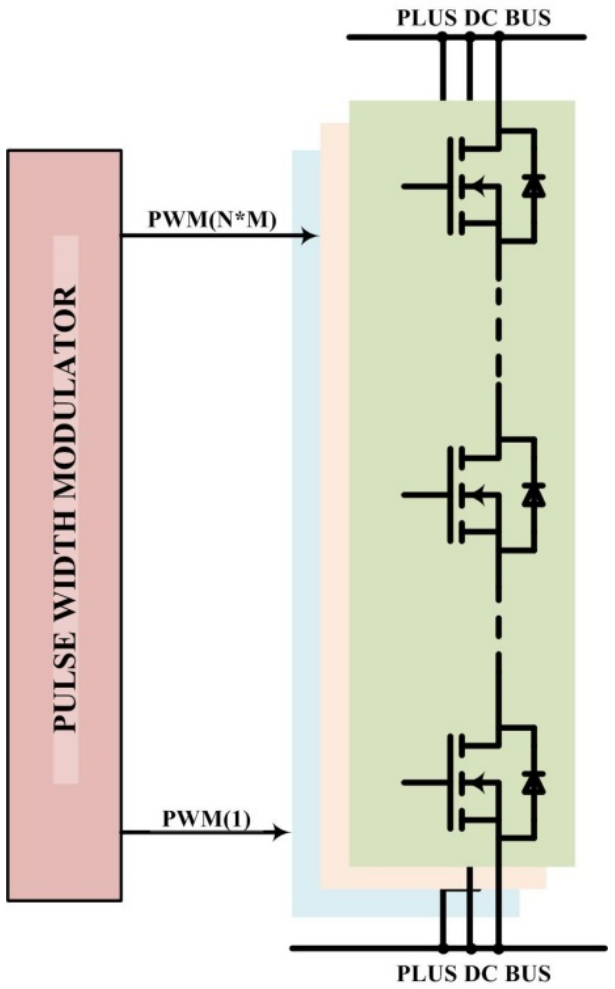




Some Issues

I. PULSE WIDTH MODULATOR

- Device=1 PWM
- 1 Converter =120 PWMs
- Traditionally *DSC TMS 335/337*
  - Max 24 PWMs
- DSC is not an Option

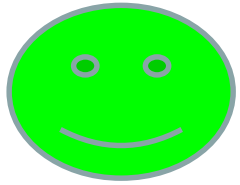


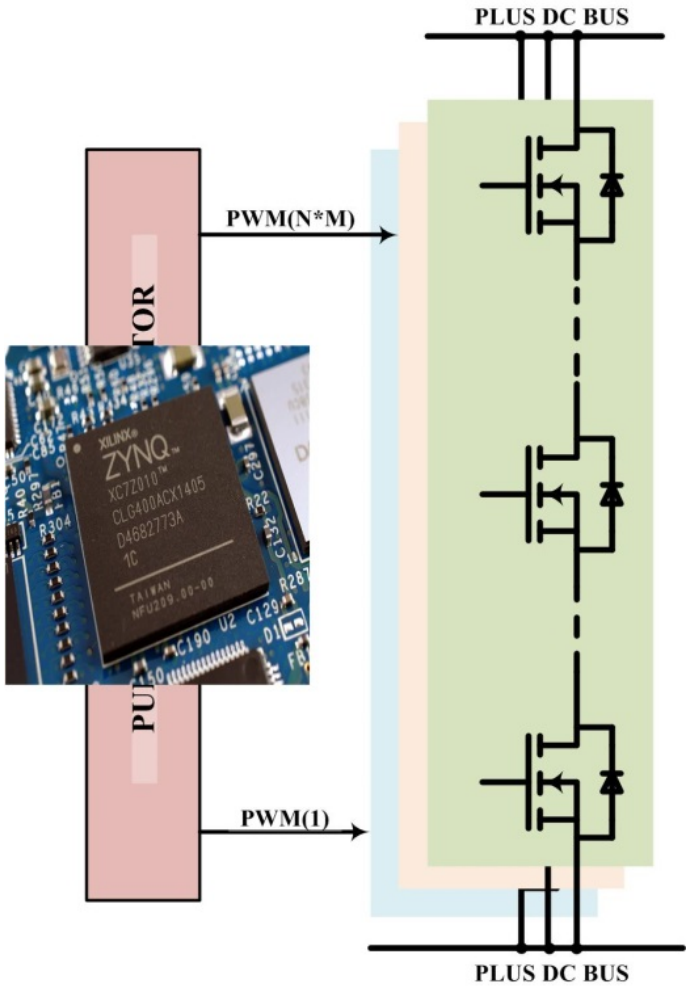
Some Issues

I. PULSE WIDTH MODULATOR

- Device=1 PWM
- 1 Converter =120 PWMs
- Traditionally *DSC TMS 335/337*
  - Max 24 PWMs

- DSC is not an Option
- Only Option is an FPGA or a CPLD

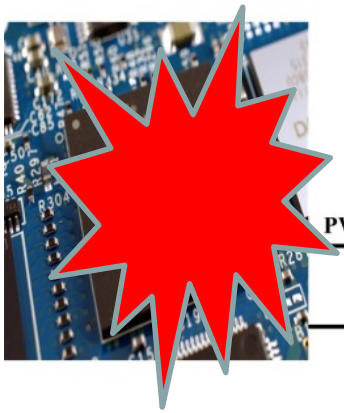


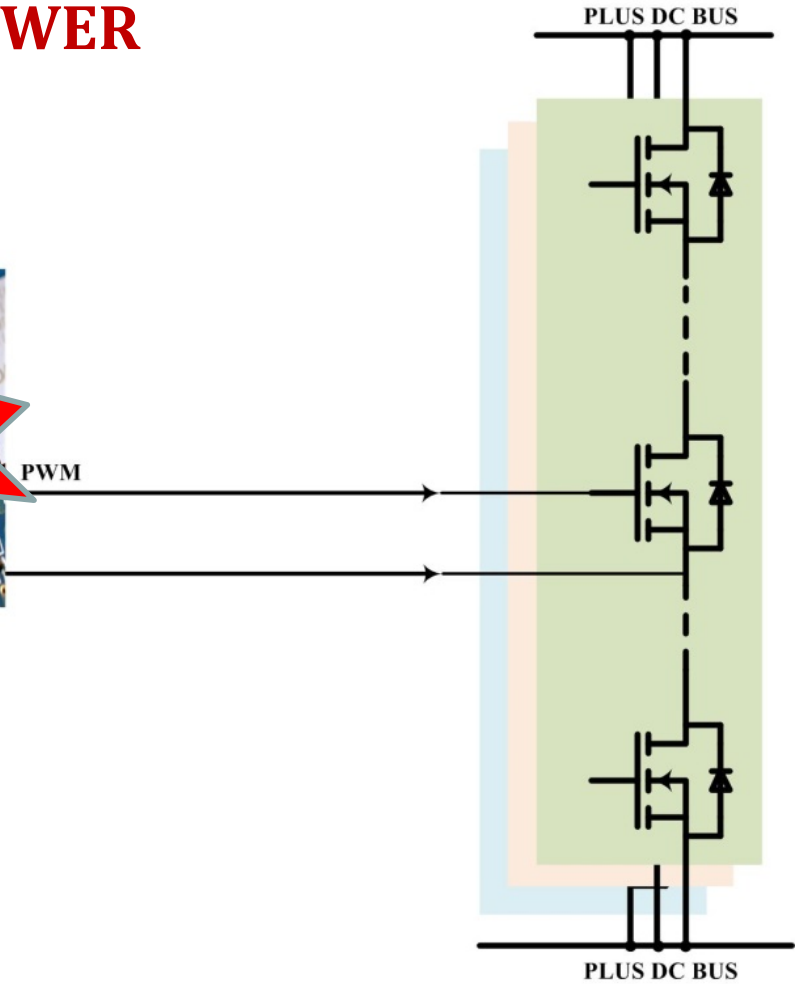


Some Issues

II. INTERFACE: CONTROL ⇔ POWER

- FPGA does not like direct connection to power device





Some Issues

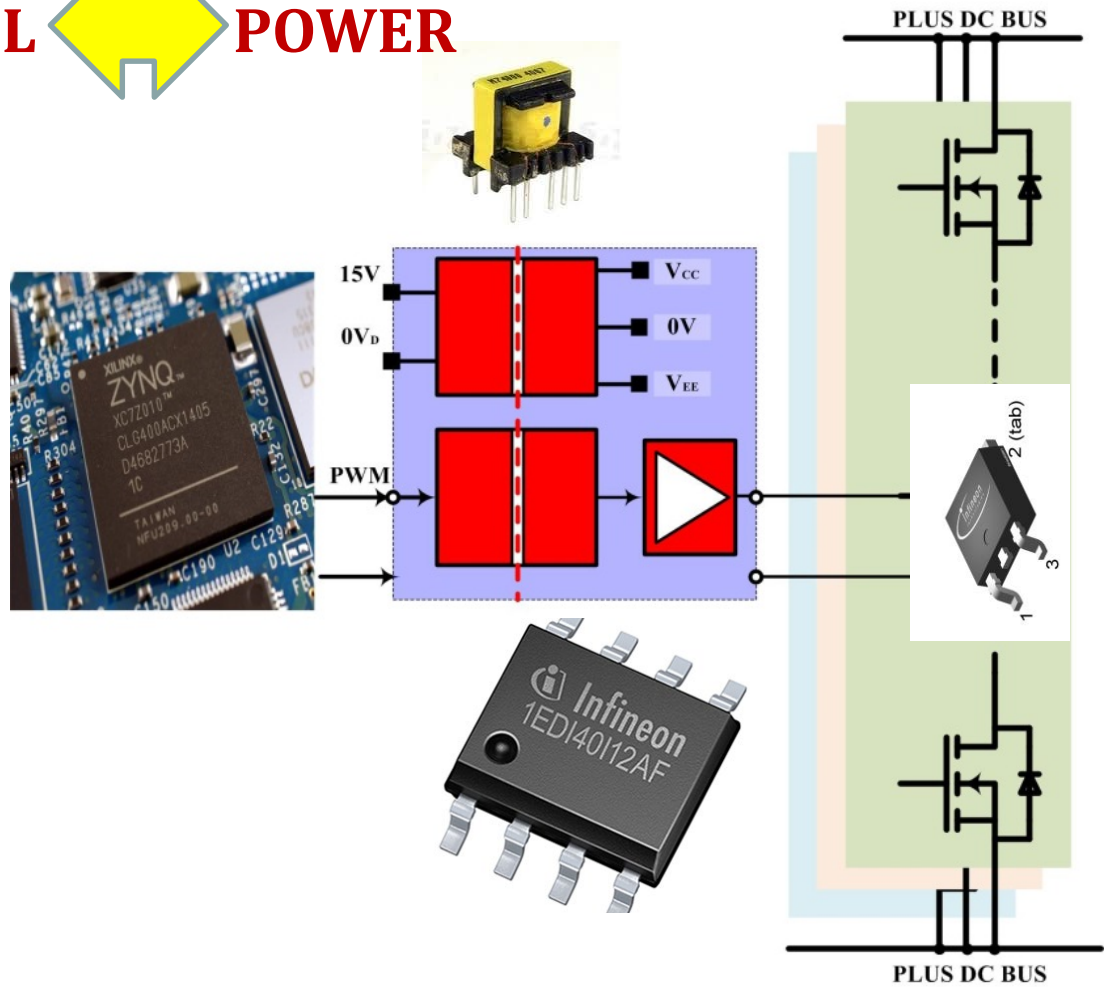
II. INTERFACE: CONTROL ⇔ POWER

- A Link between is a MUST

a) Iso.. Gate Driver,

b) Iso.. Power Supply

Today it is state of the art??



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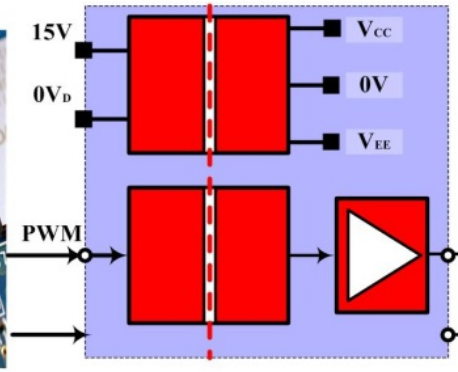
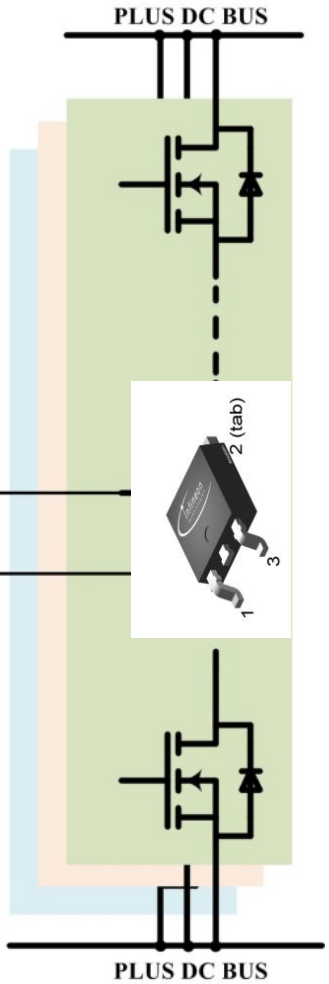
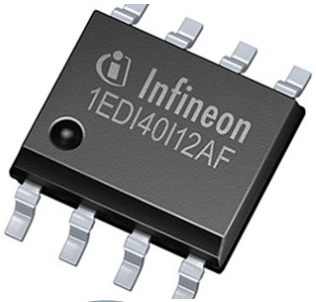






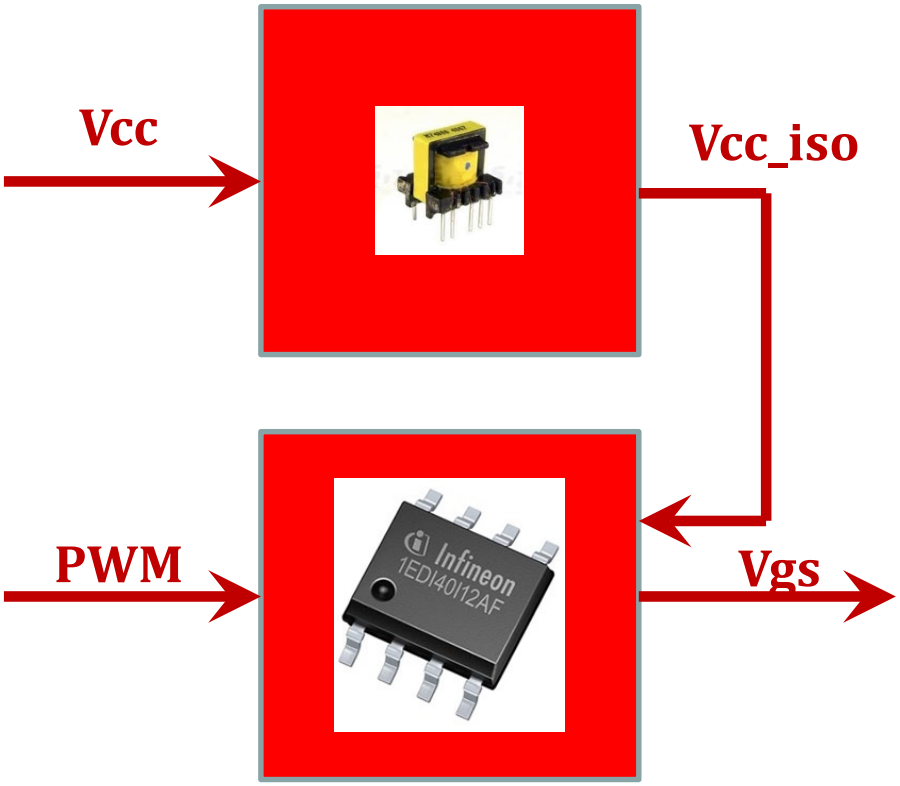
1 Device

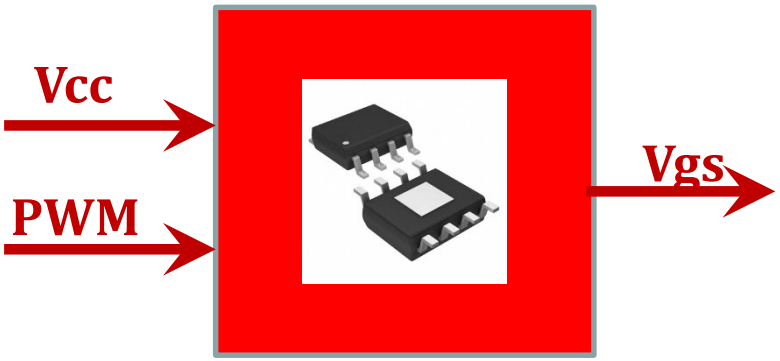
1 GD+PS

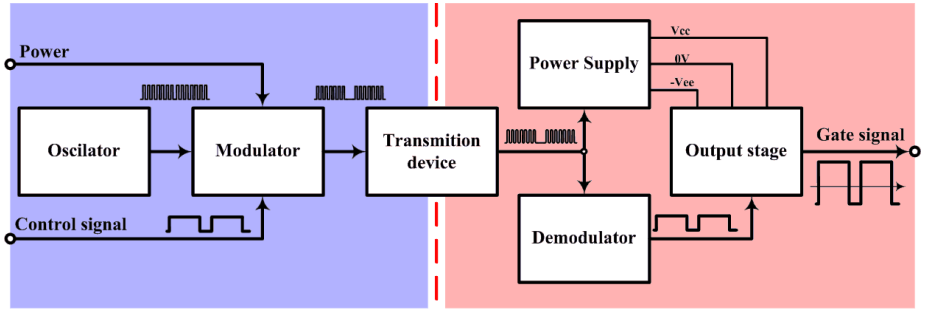
$$$$

>20% of total BOM cost

Some Issues







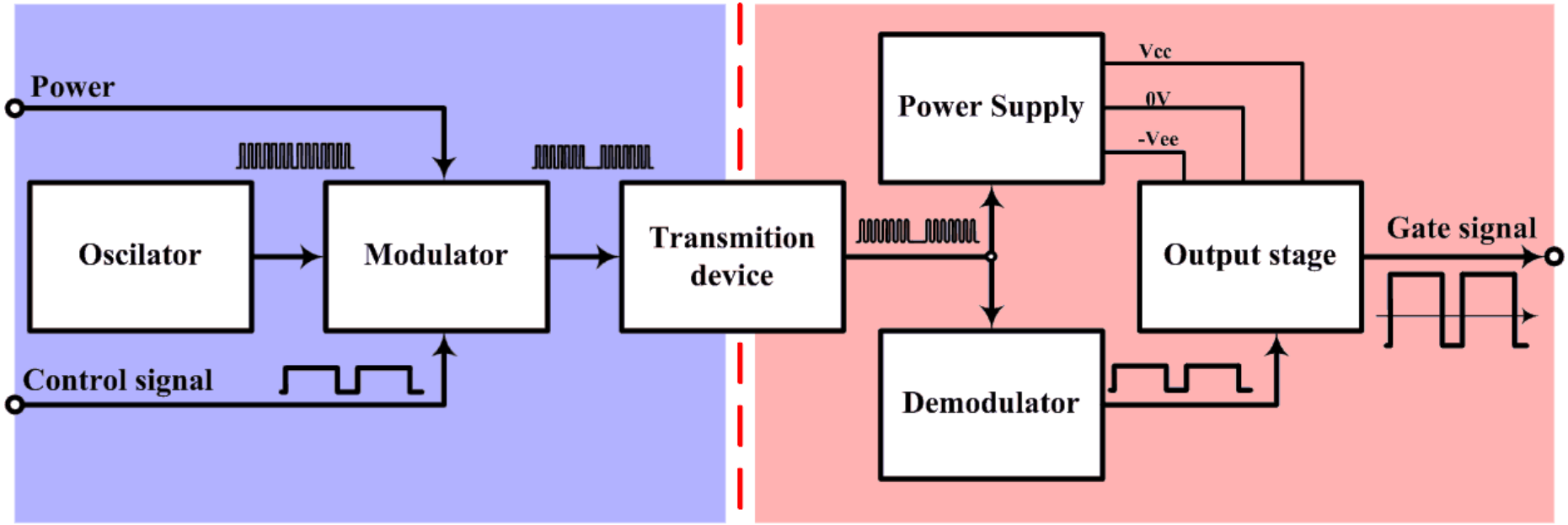
Separated Gate Driver Circuit & Power Supply

Toady

Integrated Gate Driver Circuit & Power Supply

Tomorrow

Some Issues



Integrated Gate Driver Circuit & Power Supply

- Transfer power and signal using same transmission device
  - >20MHz carrier
  - Up to 100mW power
  - Very challenging, requires very advanced manufacturing capability

Conclusion

- **There is no a magic topology that will solve all our problems!**
- **There are no new topologies, all we use today and will use tomorrow is well known since long, long time ago!**
- **We need to explore existing topologies and use them in different way:**
  - **a) Partial Power Processing Converters**
  - **b) Current Source Converters**
  - **c) Multi-Level & Multi-Cell Topologies**
  - **d) Quantum Mode Resonant Converters**

Thank you for your time

In case of any qustion, please contact me

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petar.grbovic@uibk.ac.at

www.uibk.ac.at/mechatronik/i-pel/